JEC-2701 JEC-2702



Version 1.0

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5.1 JEC-2701 8

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1.1

JEC-2701 / JEC-2702 h h
h Hu Hu h G Hu
h Hu Hu G
LGA1151 6/7/8/9 i3/i5/i7/i9/G T 35W CPU H
4 Intel (12) h H 5G 4G 5G H
PCI/PCIe/Mini PCIe h h H 6COM, 10 H8
H4 USB3.0, 4 USB2.0,1 H VGA/DVI/HDMI
G h h H Hu Hu
Hu Hu Hu Hu Hu G

1.2

	- JEC-2701	- JEC-2702
	- BOX	
	- LGA1151 6/7/8/9 i3/i5/i7/i9/G T 35W CPU	
	- H110/C236 (C236 E3 V5&V6 CPU, , SATA Raid)	
	- 2 260Pin DDR4 SO-DIMM 16GB 32GB CPU, DDR4-2133, DDR4-2400, DDR4-2666	
	- Intel CPU (CPU)	
	- VGAHuDVI-DHuHDMI H110 /C236	
	- 2 SATA3.0, SATA (C236 Raid0, 1), 1 mSATA - 1 M.2 2242/2280 SATA SSD (C236 nVME x4)	
	- Audio IC: Realtek ALC897 - Audio-Out, Mic-in, Line-out	
	- LAN IC: 1 I219LM, 3 I210AT - 4 RJ45	
USB	- 4 USB3.0 ( ), 4 USB2.0 ( ), 1 USB2.0Type A ( )	
eSPI/LPC/ SMBUS/I2C	- 1 4Pin SM Bus , LPC TPMHuTCM Hu	

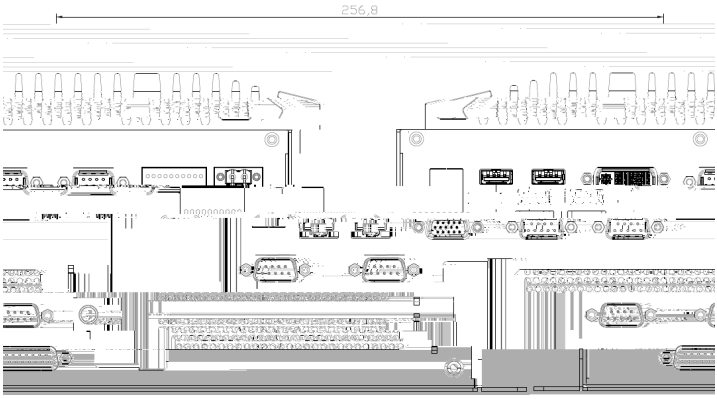
3

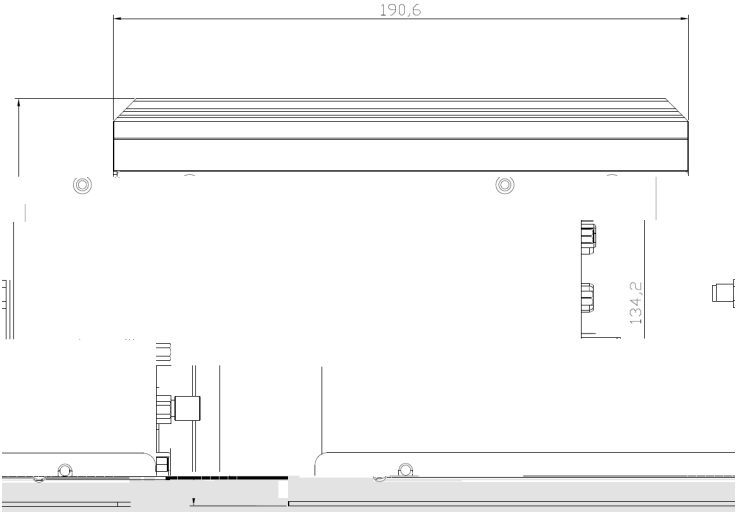
3.1

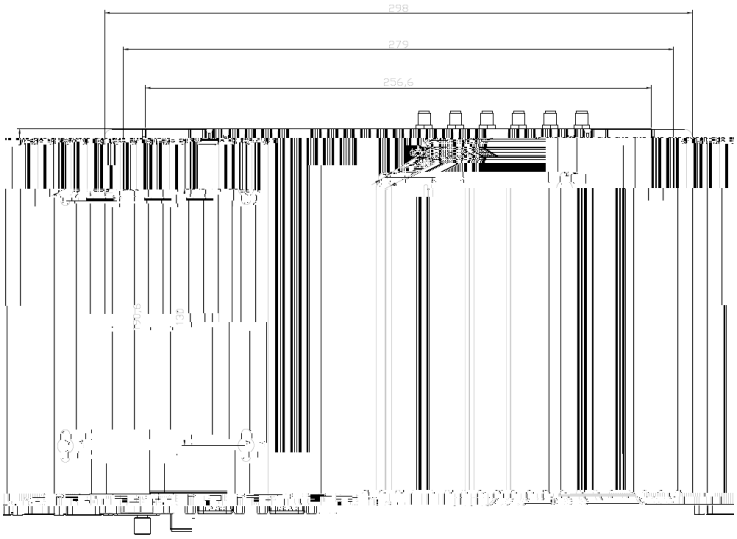
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3.2

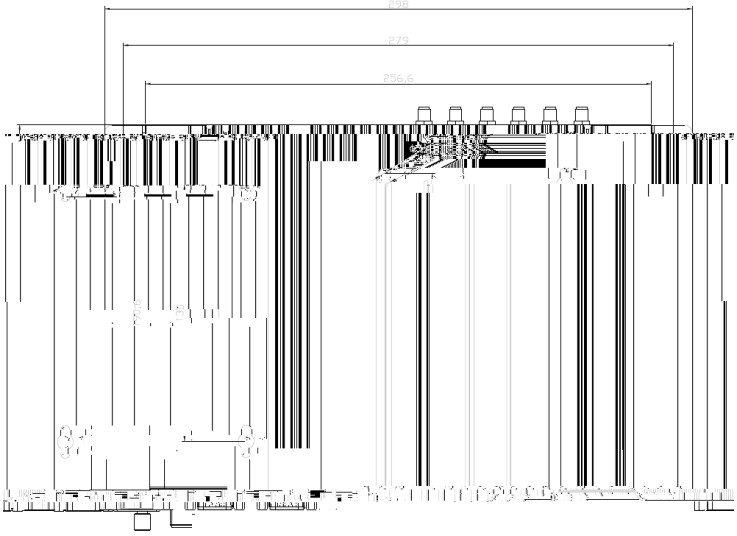
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3.3



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4.1

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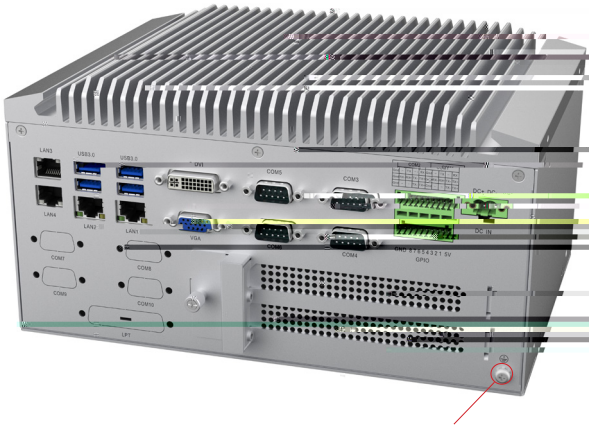
⚠
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G h I/O Ÿ USB ÿ G I/O G

4.2

Hυ I/O

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ÿ Hυ ÿ G 2.5mm2 h 0.1Ç G	

4.3

DCIN h / ч 220VAC/50Hz G	

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5

5.1 JEC-2701





5.1.1 JEC-2701 IO

5.2 JEC-2702

5.2.1JEC-2702 IO

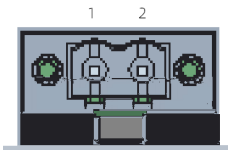
1. LAN: RJ45
2. USB3.0: USB3.0
3. VGA: VGA
4. DVI:
5. COM:
6. : COM1/2 h GPIO
7. DC_IN ч DC
8. RESET: Ў h h 4 h CMOS ў
9. L_IN:
10. L_OUT:
11. MIC_IN:
12. KB/MS:
13. HDMI: HDMI
14. SIM: SIM
15. USB2.0: USB2.0
16. LED:
17. SW:
18. Power Button: Ў ч / ҉ ў
19. ANT: WIFI

5.3

		LED	
POWER	PC		
			PC
HDD			

5.4

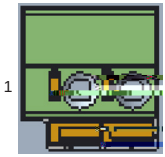
4pin Ў Ч3.5mm ў h ч



1	DC+
2	DC-

5.5

Ў h 3.5mm ч

	1	GND
	2	PWRBTN#

5.6 GPIO2 (3.5mm)

GND

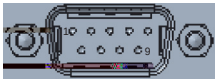
COM1/2

GPIO GND 8 7 6 5 4 3 2 1 5V

5.7 Audio

		
		L_IN
		L_OUT
		MIC_IN

5.8 COM3/4/5/6

		RS-232
	1	DCD#
	2	RXD
	3	TXD
	4	DTR#
	5	GND
	6	DSR#
	7	RTS#
	8	CTS#
	9	RI#

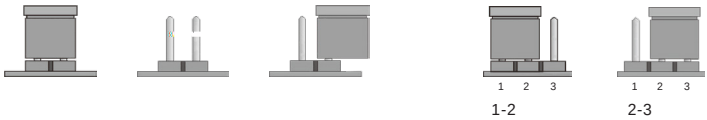
5.9

5.9.1

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1-2 2-3

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1. h "1" 1 ɢ
2. h ɢ

5.9.2

JBAT

2-3	CLEAR CMOS
1-2	NORMAL

JME

OPEN	Enable ME
CLOSE	Disable ME

5.9.3 JLPC1

1	AD3	2	+3.3V
3	AD2	4	PLTRST
5	AD1	6	FRAME
7	AD0	8	CLK
9	SERIRQ	10	GND
11	+3.3V	12	+5V

5.9.4 SATA_PWR1/2 SATA

1	+5V	2	GND
3	GND	4	+12V

5.9.5 LPT1

5.9.6 JSPK1

5.9.9 LVDS1 LVDS

1	VCC	2	VCC
3	VCC	4	GND
5	GND	6	GND
7	CHA_D0-	8	CHA_D0+
9	CHA_D1-	10	CHA_D1+
11	CHA_D2-	12	CHA_D2+
13	GND	14	GND
15	CHA_CLK-	16	CHA_CLK+
17	CHA_D3-	18	CHA_D3+
19	CHB_D0-	20	CHB_D0+
21	CHB_D1-	22	CHB_D1+
23	CHB_D2-	24	CHB_D2+
25	GND	26	GND
27	CHB_CLK-	28	CHB_CLK+
29	CHB_D3-	30	CHB_D3+

JLVDS (
LVDS/EDP

1-2	3.3V
2-3	5V

LVDS

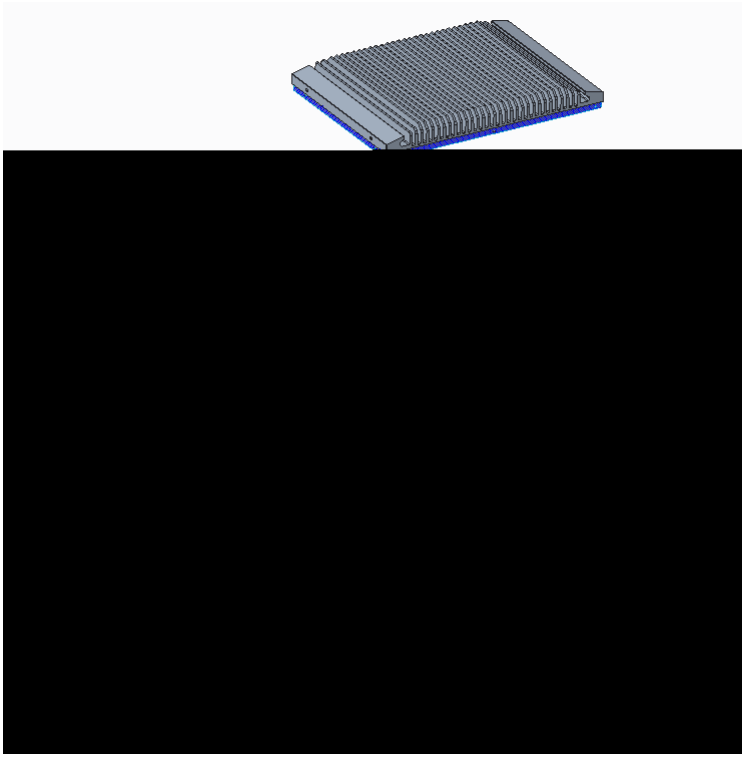
5.9.10 EDP EDP

1	BKL_PWR	2	BKL_PWR
3	BKL_PWR	4	GND
5	GND	6	NC
7	KEY	8	NC_SCL
9	LCD_VCC	10	NC_SDA
11	LCD_VCC	12	

EDP

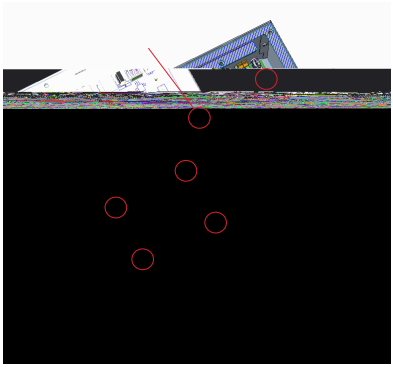
6

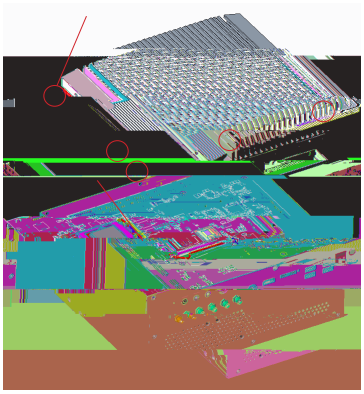
6.1



1		2		3	
4		5			

6.2 CPU



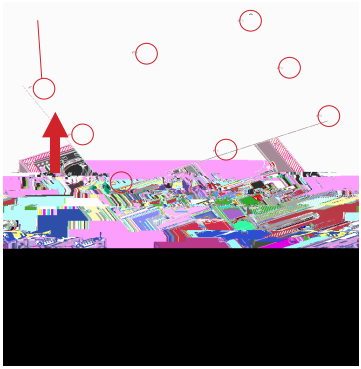


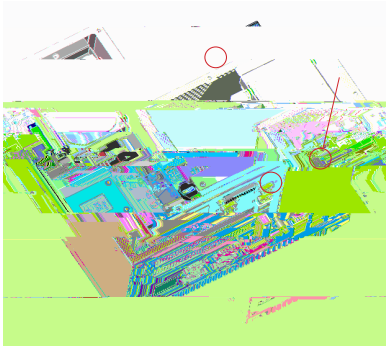
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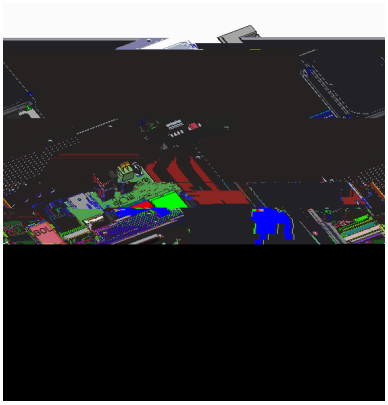
1. 10 6#32*5 h Ђ
2. 10 M3 Ђ
3. 10 6#32*5 h Ђ
4. h CPU h CPU h G

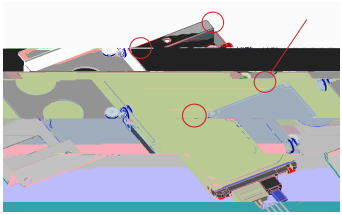
ч 1. CPU h CPU h CPU Ђ
2. CPU CPU h G

6.3

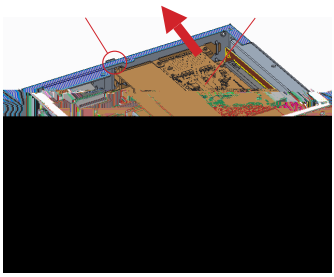








6.4

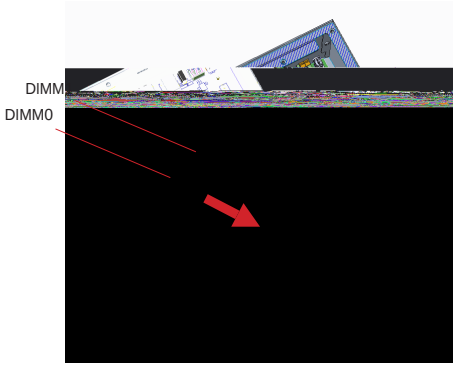


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6.5



ч DIMM h ɢ

ч 1. h h
h Ӈ
2. h Ӈ
3. h DIMM1 h DIMM0 Ӈ
4. h DIMM0 DIMM1 30° ɢ

6.6 M.2 2242/2280

ч M.2 1 M2 h M.2 2242/2280 SATA SSD G

6.8 WIFI



ч WIFI g

ч WIFI h 30° g

7 BIOS

7.1 BIOS

AMI BIOS ɢ BIOS Basic Input Output System (ÿ ɢ
ROM Ÿ Read-Only Memory) ɢ h BIOS
h ч
a. h POST(Power On Self Test) ɢ
b. ɢ
c. Hʊ ɢ
d. SETUP ɢ
BIOS CMOS RAM h
ɢ h h BIOS ɢ CMOS
h BIOS ɢ

7.2 BIOS

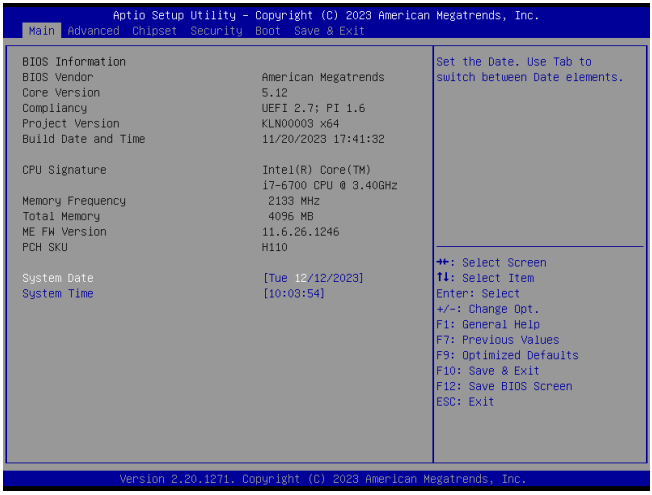
BIOS Setup h ɢ BIOS
h h h ɢ
SETUP ч
a. h SETUP ʜ
b. ċ ɢ

BIOS BIOS

7.3 BIOS

Main		BIOS
Advanced		BIOS
Chipset		
Security		
Boot		
Save & Exit		BIOS

7.4 Main



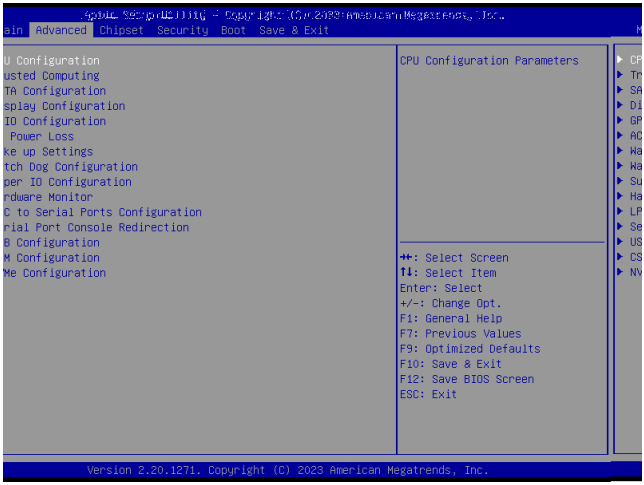
System Date ( )

, d , / / d G

System Time

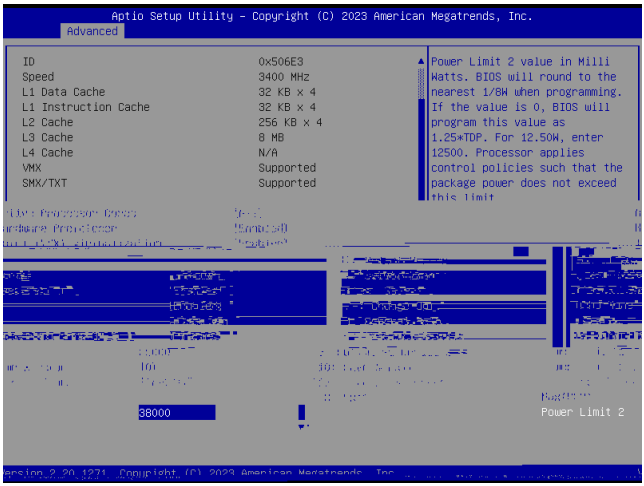
< >< >< > G

7.5 Advanced



CPU Conżguration	CPU	
Trusted Computing		
SATA Conżguration	SATA	
Display Conżguration		
GPIO Conżguration	GPIO	
AC Power Loss		
Wake up Setting		
Watch Dog Conżguration		
Super IO Conżguration	I0	
Hardware Monitor		/
LPC to Serial Ports Conżguration	LPC	
Serial Port Console Redirection		
USB Conżguration	USB	
CSM Conżguration	CSM	
NVMe Conżguration	NVMe	/

CPU Conżguration <Enter> G



Active Processor Cores

G ↳ All,1.

Hardware Prefetcher

G ↳ Disable,Enable.

Intel(VMX) Virtualization Technology

Intel Ÿ VMX ÿ G ↳ Disable,Enable.

Hyper-Threading

G ↳ Disable,Enable.

Intel(R) Speedstep(tm)

G ↳ Disable,Enable.

Turbo Mode

G ↳ Disable,Enable.

C states

CPU G ↳ Disable,Enable.

CPU Turbo Boost Power Max(PL1)

CPU Ÿ PL1 ÿ G ↳ Disable,Enable.

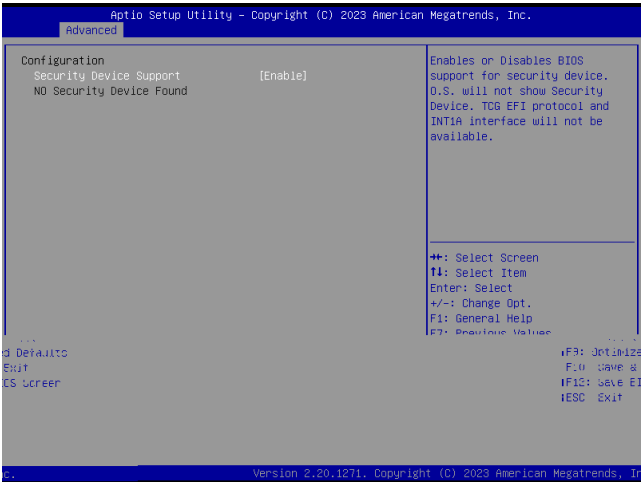
Power Limit 1 Time Window

1 G ↳ 1,2,3,4,5,6,7,8,9,10,12,14,16,20,24,28,32,40,48,56,64,80,96,112,128.

CPU Turbo Boost Power Max(PL2)

CPU Ÿ PL2 ÿ G ↳ Disable,Enable.

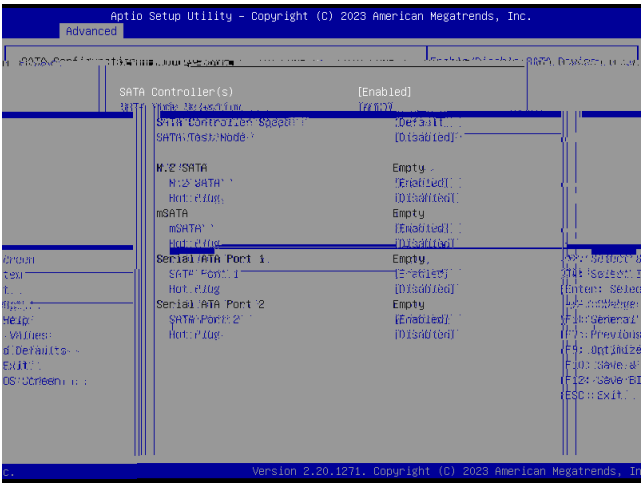
Trusted Computing <Enter> ɢ



Security Device Support

BIOS ɢ ɥ Disable,Enable.

SATA Conžguration <Enter> ɢ



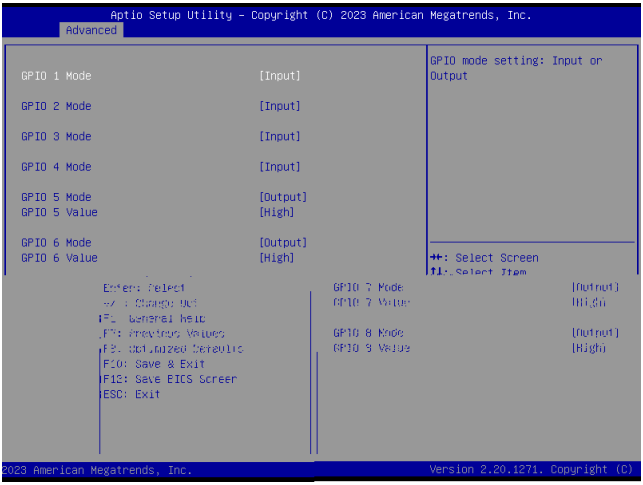
SATA Controller(s)

SATA ɢ ɥ Disable,Enable.

SATA Mode Selection

SATA ɢ ɥ AHCI.

GPIO Conżguration <Enter> G



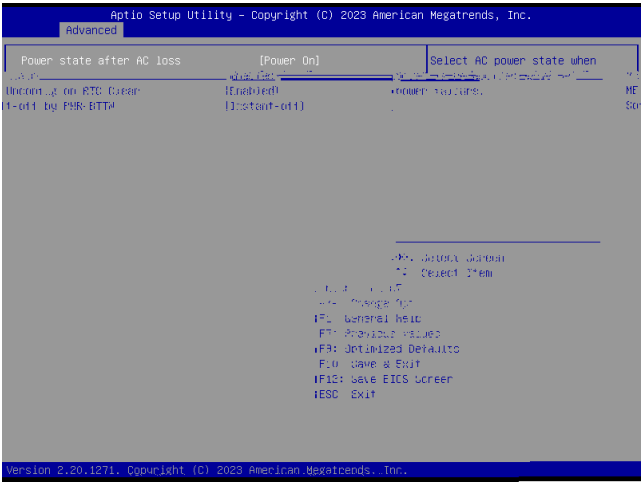
GPIO 1/2/3/4/5/6/7/8 Mode

GPIO G ч Input,Output.

GPIO 1/2/3/4/5/6/7/8 Value

GPIO G ч Low,High.

AC Power Loss <Enter> G



Power state after AC loss

G ч Power On,Power Ob,Last State.

ME state

ME G ч Disable,Enable.

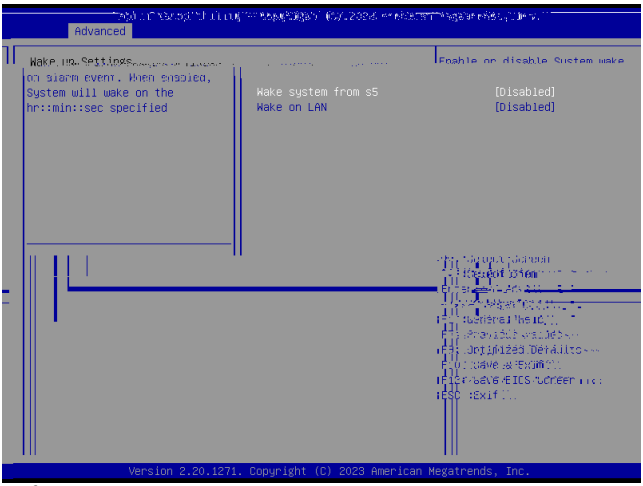
ME Uncon f g On RTC Clear

ME G ч Disable,Enable.

Soft-o f by PWR-BTTN

G ч Delay 4 sec,Instant-oƀ.

ʒ Wake up Settings <Enter> G



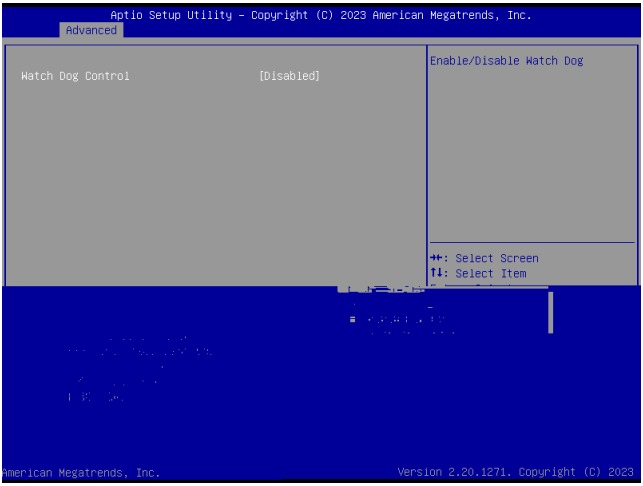
Wake system form s5

s5 G ч Disable,Fixed Time,Dynamic Time.

Wake on LAN

G ч Disable,Enable.

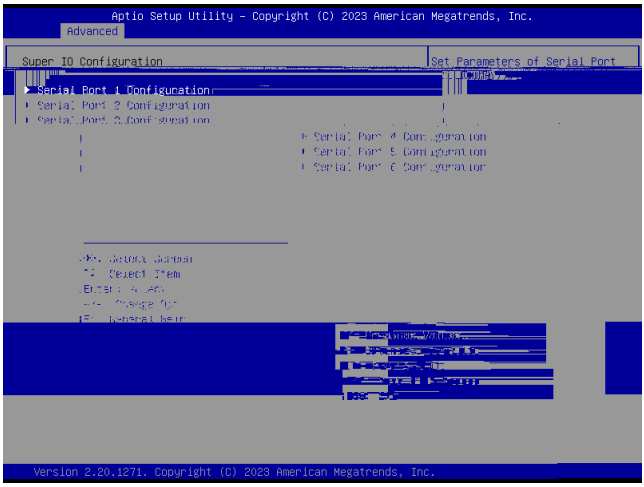
Watch Dog Conžguration <Enter> G



Watch Dog Control

G ч Disable,Enable.

Super IO Conžguration <Enter> G



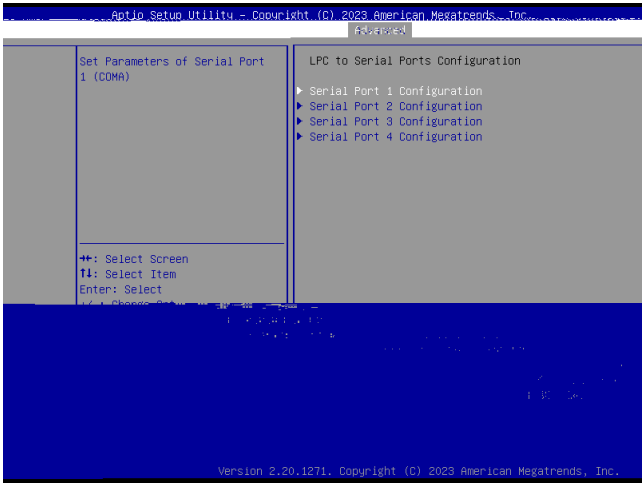
Serial Port 1/2/3/4/5/6 Con f guration

G

Parallel Port Con f guration

G

y LPC to Serial Ports Conžguration <Enter> G



Legacy USB Support

USB G ↳ Disable,Enable,Auto.

XHCI Hand-o f

XHCI G ↳ Disable,Enable.

USB Mass Storage Driver Support

USB G ↳ Disable,Enable.

Port 60/64 Emulation

60/64 G ↳ Disable,Enable.

USB transfer time-out

USB G ↳ 1sec,5sec,10sec,20sec.

Device reset time-out

G ↳ 10sec,20sec,30sec,40sec.

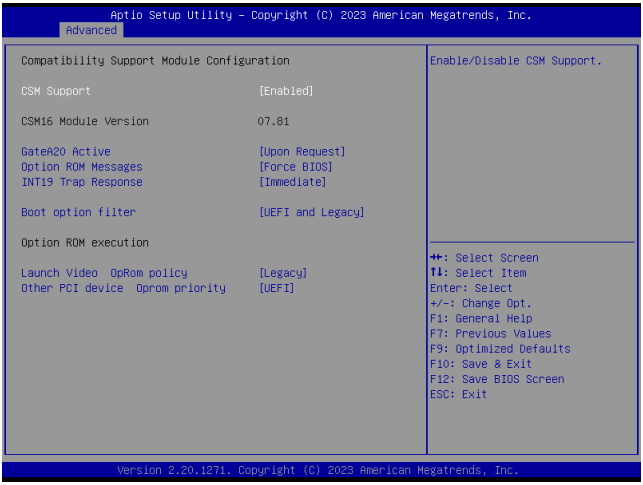
Device power-up delay

G ↳ Auto,Manual.

VendorCoProductCode 2.00

G ↳ Auto,Floppy,Forced FDD,Hard Disk,CD-ROM.

y CSM Conžguration <Enter> G



CSM Support

CSM G ↳ Disable,Enable.

GateA20 Ative

20 G ↳ Upon Request,Always.

Option ROM Messages

ROM G ↳ Force BIOS,Keep Current.

INT19 Trap Response

INT19 G ↳ Immediate,Postpond.

Boot option fIter

G ↳ UEFI and Legacy,Legacy only,UEFI only.

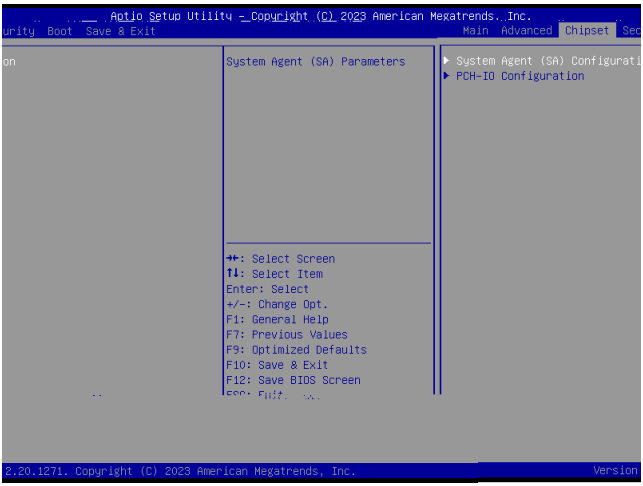
Launch Video Oprom policy

G ↳ Do not launch,UEFI,Legacy.

Other PCI device Oprom priority

PCI Oprom G ↳ Do not launch,UEFI,Legacy.

7.6 Chipset



System Agent Ÿ SA) Conžguration	Ÿ SA ÿ	
PCH-IO Conžguration	PCH-IO	

PCI Express Con f guration

PCI Express G

LAN Con f guration

G

USB Con f guration

USB G

HD Audio Con f guration

G

7.7 Security

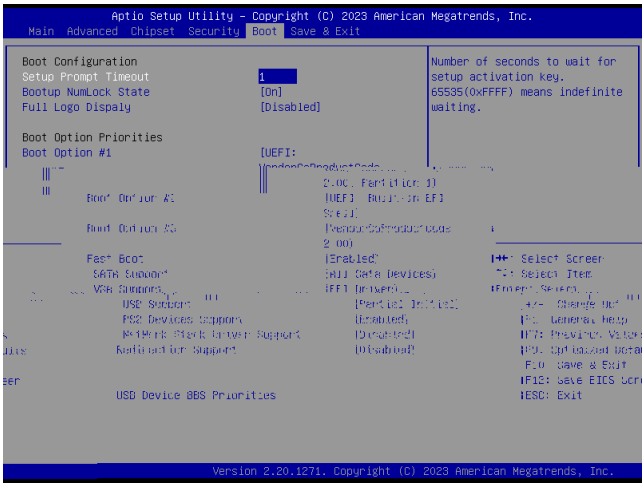


Administrator Password

h ч

1. Administrator Password h <Enter> G
2. d Create New Password d 3~20 h <Enter> h d Conžrm Password d h G d Invalid Password! d h h G h d Administrator Password d h d Enter Current Password d h d Create New Password d <Enter> G

7.8 Boot



Setup Prompt Timeout

G

Boot NumLock State

NumLock G ч On,Oъ.

Full Logo Dispaly

G ч Disable,Enable.

Boot Option #1

1 G ч Kingston Data Traveler 2.01.00,Disable.

Fast Boot

G ч Disable,Enable.

Option ROM Messages

ROM G

8 WDT

8.1

JEC-2701 / JEC-2702 WatchDog G

Ч WDT ITE8786 Super IO G

8.1.1 IO

Linux h Ч

```
#include <stdio.h>
#include <errno.h>
#include <sys/io.h>

// IO 1 Byte
/*
    Name:IoRead8
    Input: GpioAddress - GPIO base address
    Output: GPIO port read value
    Description:
*/
unsigned char IoRead8(unsigned short GpioAddress) {

    unsigned char ret;

    ret = iopl(3);

    if (ret)

    {
        printf("ret = %d\n", ret);

        printf("errno = %d\n", errno);

        printf("error for iopl\n");

        return 1;

      }

   return inb(GpioAddress);
```

```
}

    //    IO          1    Byte
unsigned char IoWrite8(unsigned short GpioAddress, unsigned char Data) {
    unsigned char ret;

    ret = iopl(3);

    if (ret)

    {
            printf("ret = %d\n", ret);
```

//h. Super lO Conžguration Mode

loWrite8(SuperlO_lndex_Port, 0x02);

loWrite8(SuperlO_lndex_Port, 0x02);// Super lO Conžguration Mode h //SuperlO

, Conžguration Mode ɢ

9 GPIO

9.1

JEC-2701 / JEC-2702 GPIO G
Ч GPIO Intel PCH h GPIO
G h GPIO G

9.1.1 BIOS

```
/**
  Reads a 32-bit MMIO register.

  Reads the 32-bit MMIO register specižed by Address. The 32-bit read value is
  returned. This function must guarantee that all MMIO read and write
  operations are serialized.

  If Address is not aligned on a 32-bit boundary, then ASSERT().

  If 32-bit MMIO register operations are not supported, then ASSERT().

  @param  Address The MMIO register to read.

  @return The value read.

**/
UINT32
EFIAPI
MmioRead32 (
  IN      UINTN                     Address
  )
{
  //
  // Make sure Address is aligned on a 32-bit boundary.
  //
  ASSERT ((Address & 3) == 0);
  return (UINT32)MmioReadWorker (Address, EžCpuIoWidthUint32);
}

/**

Writes a 32-bit MMIO register.

Writes the 32-bit MMIO register specižed by Address with the value specižed
```

```
  by Value and returns Value. This function must guarantee that all MMIO read
  and write operations are serialized.

  If Address is not aligned on a 32-bit boundary, then ASSERT().

  If 32-bit MMIO register operations are not supported, then ASSERT().

  @param  Address The MMIO register to write.
  @param  Value   The value to write to the MMIO register.

**/
UINT32
EFIAPI
MmioWrite32 (
  IN     UINTN                 Address,
  IN     UINT32                Value
  )
{
  //
  // Make sure Address is aligned on a 32-bit boundary.
  //
  ASSERT ((Address & 3) == 0);
  return (UINT32)MmioWriteWorker (Address, EfiCpuIoWidthUint32, Value);
}
/**
  Reads memory-mapped registers in the EFI system memory space.

  Reads the MMIO registers specified by Address with registers width specified by Width.
  The read value is returned. If such operations are not supported, then ASSERT().
  This function must guarantee that all MMIO read and write operations are serialized.

  @param  Address      The MMIO register to read.
                       The caller is responsible for aligning the Address if required.
  @param  Width        The width of the I/O operation.
  @return Data read from registers in the EFI system memory space.

**/
UINT64
EFIAPI
MmioReadWorker (
  IN     UINTN                  Address,
  IN     EFI_CPU_IO_PROTOCOL_WIDTH  Width
```

```
  ASSERT_EFI_ERROR (Status);

  return Data;
}
```

9.2 GPIO

9.2.1 8 GPIO

GPIO1 ч 0xFDAE0638/0xFDAE0580(AIoT0-H110 only)
GPIO2 ч 0xFDAE0588
GPIO3 ч 0xFDAE0590
GPIO4 ч 0xFDAE05E8
GPIO5 ч 0xFDAE05F0
GPIO6 ч 0xFDAE05F8
GPIO7 ч 0xFDAE0600
GPIO8 ч 0xFDAE0608

9.2.2 GPIO1

UINT Data32 Ц

GPIO
//a. GPIO1
Data32 = MmioRead32(0xFDAE0638);
MmioWrite32 Ў 0xFDAE0638 h Data32 &0xFFFFFDFF|0x00000100 ў ;

//b. GPIO1
Data32 = (MmioRead32(0xFDAE0638)&0x02)>>1;

GPIO
//a. GPIO1
Data32 = MmioRead32(0xFDAE0638);
MmioWrite32 Ў 0xFDAE0638 h Data32 &0xFFFFFEFF|0x00000200 ў ;

//b. GPIO1
Data32 = MmioRead32(0xFDAE0638);
MmioWrite32 Ў 0xFDAE0638 h Data32 &0xFFFFFFFE ў ; //

MmioWrite32 Ў 0xFDAE0638 h Data32 |0x01 ў ; //

//c. GPIO1
Data32 = (MmioRead32(0xFDAE0638)&0x01) Ц
GPIO h GPIO G

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11

11.1

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		G h
		1Hט 2Hט 3Hט h
		ÿ ÿ Hט
		ÿ Winpe ÿ h h
lHO h		PCI ISA Hט Hט h
	BIOS	h BIOS Setup h BIOS Setup
BIOS h		
Boot device not found	BIOS h h	BIOS d d (Boot) h
USB	USB 2.0 h USB 2.0	USB 2.0
	USB	1Hט USB Legacy Support ÿ USB ÿ 2Hט h USB