

Version 1.0

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A G h G h G

G h G

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G G h G

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ESD

(ESD, electrostatic sensitive devices) Ч



ESD h Ч

- ESD h Ў h ў G
- G
- ESD h G
- ESD G
- ESD G

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2

2.1

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h h Ң Ң
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2.2

h 0œ‘ 40œ h
20%‘ 85% ɢ Ң Ң h
Ң ɢ 10cm h Ң Ң Ң
50cm ɢ

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2.3

2.3.1

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2.4

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- 50mm 100mm ɢ
- (ÿ ɢ
- ɢ
- I/O 0.5V ɢ

3

3.1

□ 19″ ■ Ÿ ÿ □
□ □ VESA □
□ _____

3.2

ч mm

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4.1

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4.2

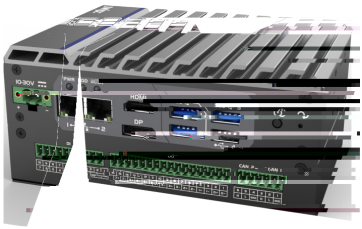
DCIN h h DCIN G	DC IN

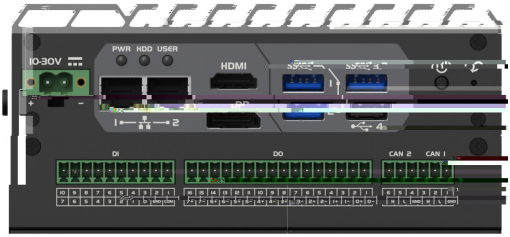
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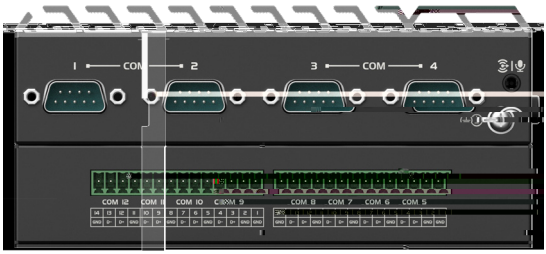
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5

5.1

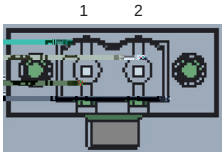




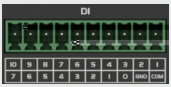


1. DC_IN ч DC
2. LAN: RJ45
3. PWR:

5.4

		
	1	DC+
	2	DC-

5.5 DI

										
	1	2	3	4	5	6	7	8	9	10
	COM	GND	DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7

5.6 DO

										
	1	2	3	4	5	6	7	8	9	10
	DO-	DO+	D1-	D1+	D2-	D2+	D3-	D3+	D4-	D4+
	11	12	13	14	15	16				
	D5-	D5+	D6-	D6+	D7-	D7+				

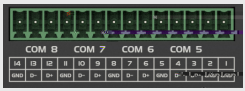
5.7 CAN1/2

						
	CAN1			CAN2		
	1	2	3	4	5	6
	GND	L	H	GND	L	H

5.8 COM1/2/3/4

COM1/2/3/4 RS232/422/485 BIOS

5.9 COM5/6/7/8



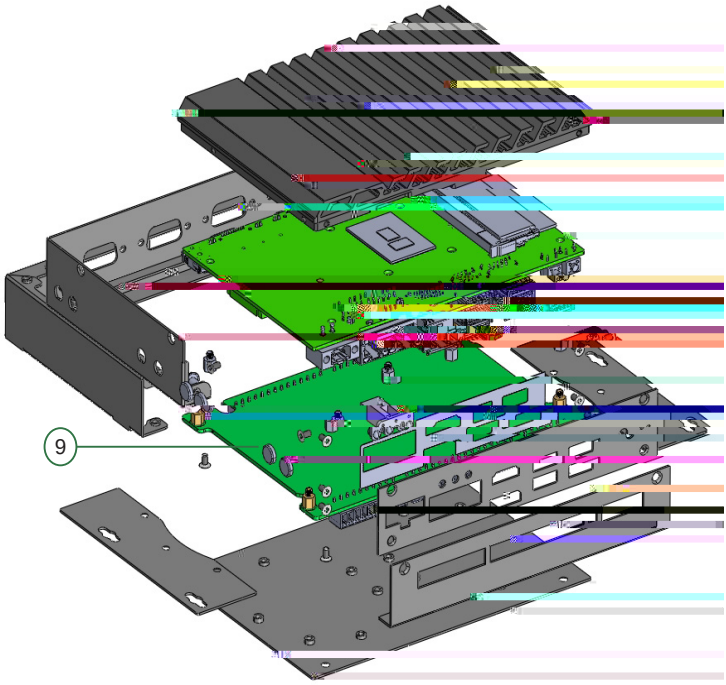
	1	2	3	4	5	6	7
	GND	GND	D+	D-	GND	D+	D-
	8	9	10	11	12	13	14
	GND	D+	D-	GND	D+	D-	GND

5.10 COM9/10/11/12

	1	2	3	4	5	6	7
	GND	GND	D+	D-	GND	D+	D-
	8	9	10	11	12	13	14
	GND	D+	D-	GND	D+	D-	GND

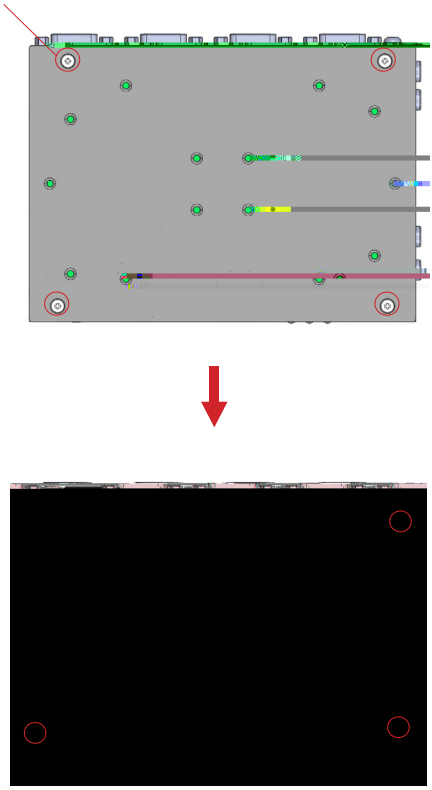
6

6.1



1		2		3	CPU
4		5		6	IO
7	IO	8		9	
10		11			

6.2



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1. 4 h Ь
2. 4 h g

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ⅾ 6.2 d h ч

1. 8 4 h Ꮒ
2. DIMM h ɢ

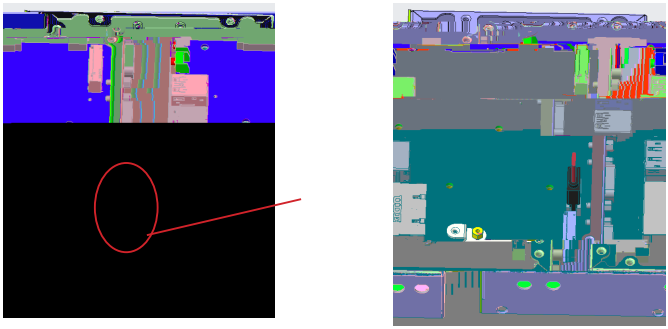
ч 1. h 30° h h Ꮒ
2. M.2 2242 h M.2 2280 M.2 2242 ɢ

6.5 4G/5G



ч 4G/5G ɢ
4G/5G h 30° ɢ

ч 4G h 4G ɢ



7 BIOS

7.1 BIOS

AMI BIOS ɢ BIOS Basic Input Output System (ÿ ɢ
ROM Ÿ Read-Only Memory) ɢ h BIOS
h ч
a. h POST(Power On Self Test) ɢ
b. ɢ
c. Hʊ ɢ
d. SETUP ɢ
BIOS CMOS RAM h
ɢ h h BIOS ɢ CMOS
h BIOS ɢ

7.2 BIOS

BIOS Setup h ɢ BIOS
h h h ɢ
SETUP ч
a. h SETUP Ь
b. ɢ

ч BIOS h h BIOS ɢ
ɢ

7.2.1 BIOS

h h <DEL> BIOS
ɢ

Press <Delete> to enter SETUP

Press <F11> to enter Boot Menu

7.2.2

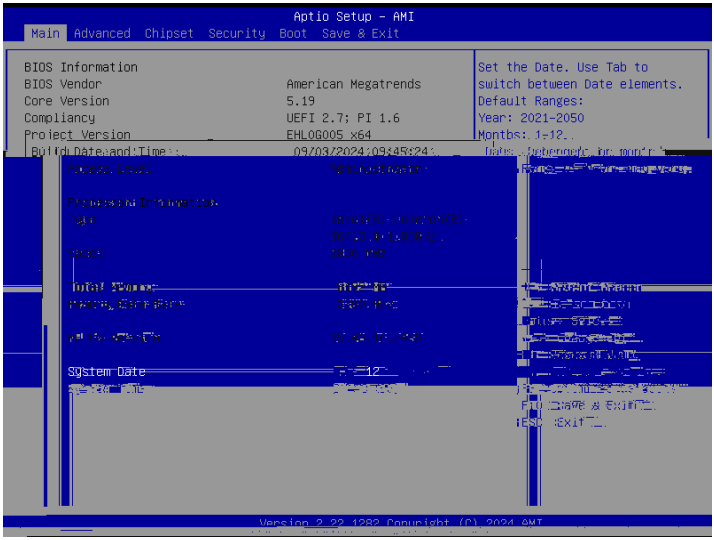
h <Enter> h <F1> h <Esc>
ɢ ɢ

/	
/	
+/ -	/
<Enter>	h
<ESC>	h CMOS SETUP
<F1>	
<F7>	
<F9>	
<F10>	CMOS

7.3 BIOS

Main		BIOS
Advanced		BIOS
Chipset		
Security		
Boot		
Save & Exit		BIOS

7.4 Main



System Date ( )

, d , / / d G

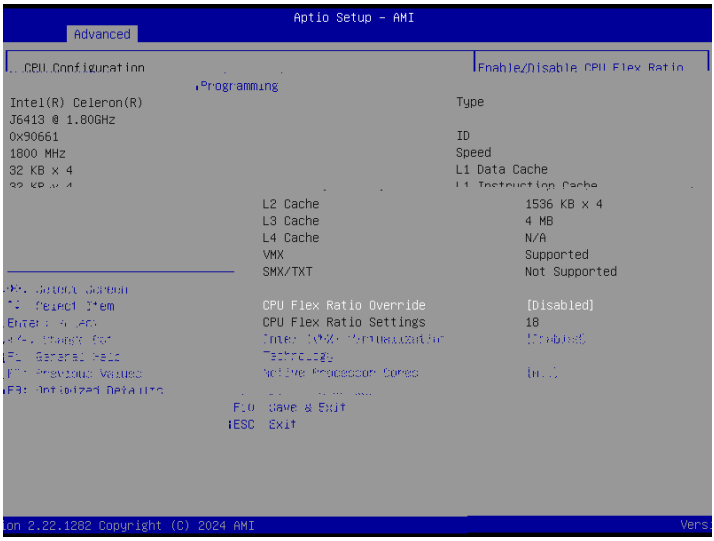
System Time

< >< >< > G

7.5 Advanced

CPU Configuration	CPU	
CPU Performance Configuration	CPU	
Trusted Computing		
Watch Dog Configuration		
Super IO Configuration	Super IO	
Hardware Monitor		
Power Management Configuration		
Serial Port Console Redirection		
AMI Graphic Output Protocol Policy		

CPU Con f guration <Enter> G



CPU Flex Ratio Override

CPU G

ч Disable,Enable.

. Intel(VMX) Virtualization Technology

Intel Ÿ VMX ÿ G

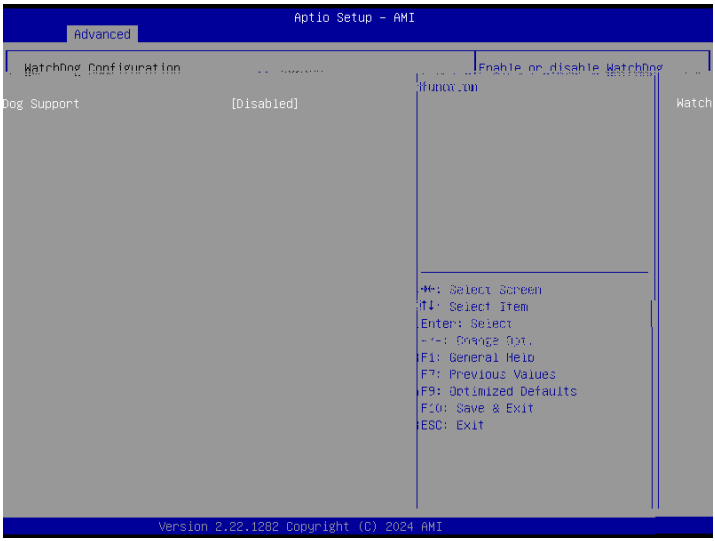
ч Disable,Enable.

Active Processor Cores

G

ч ALL,1,2,3.

Watch Dog Con f guration <Enter> G



WatchDog Support

G

ч Disable,Enable.

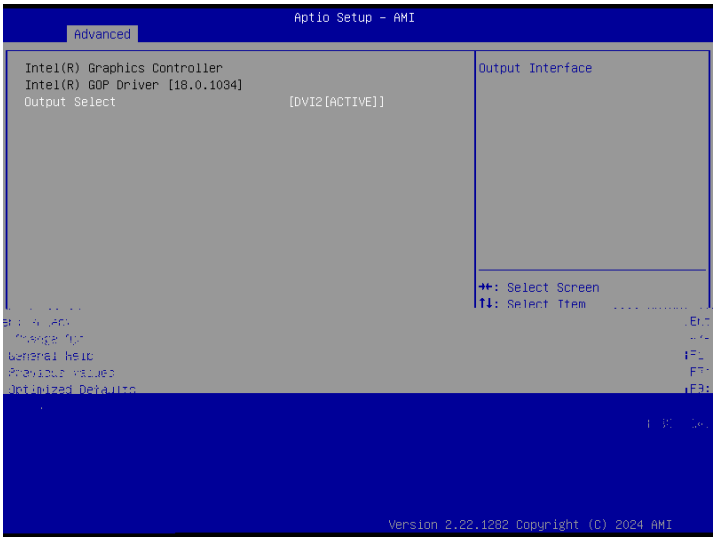
Super IO Con f guration <Enter> G



Serial Port 1/2/3/4 Con f guration

G

AMI Graphic Output Protocol Policy <Enter> G

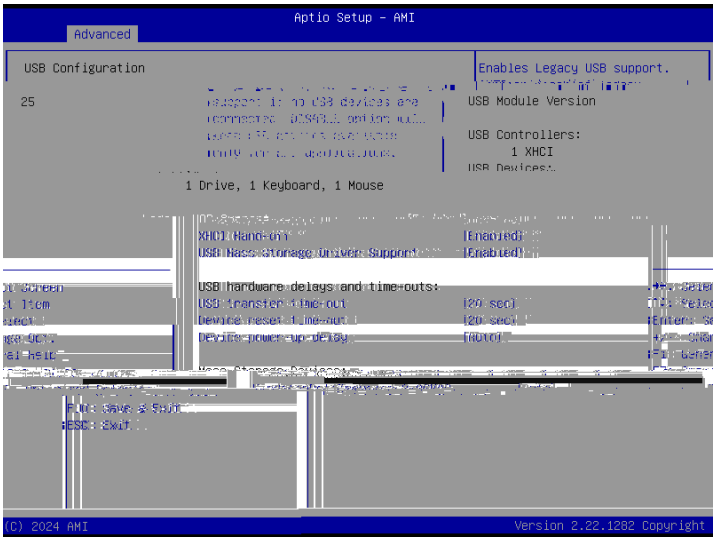


Output Select

G

ч DVI2[ACTIVE].

USB Conf guration <Enter> G



Legacy USB Support

USB G

↳ Disable,Enable,Auto.

XHCI Hand-of f

XHCI G

↳ Disable,Enable.

USB Mass Storage Driver Support

USB G

↳ Disable,Enable.

USB transfer time-out

USB G

↳ 1sec,5sec,10sec,20sec.

Device reset time-out

G

↳ 10sec,20sec,30sec,40sec.

Device power-up delay

G

↳ Auto,Manual.

Network Stack Confguration <Enter> G

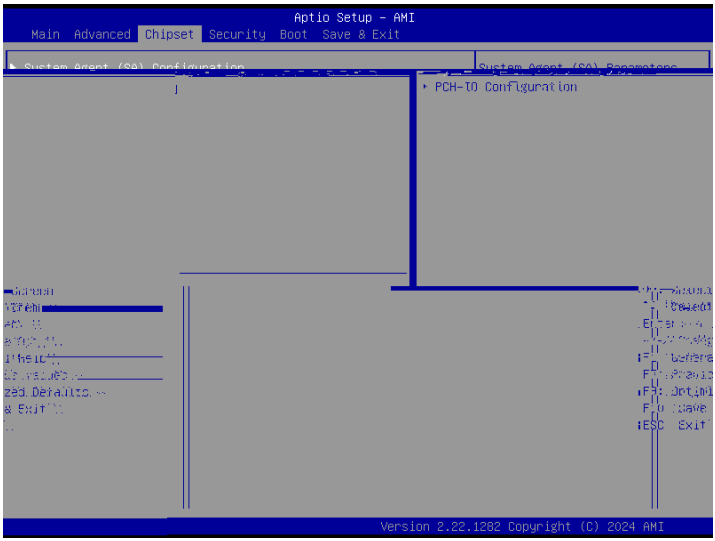


Network Stack

G

↳ Disable,Enable.

7.6 Chipset



System Agent Ÿ SA) Con f guration	Ÿ SA ÿ	
PCH-IO Con f guration	PCH-IO	

HD Audio Con f guration

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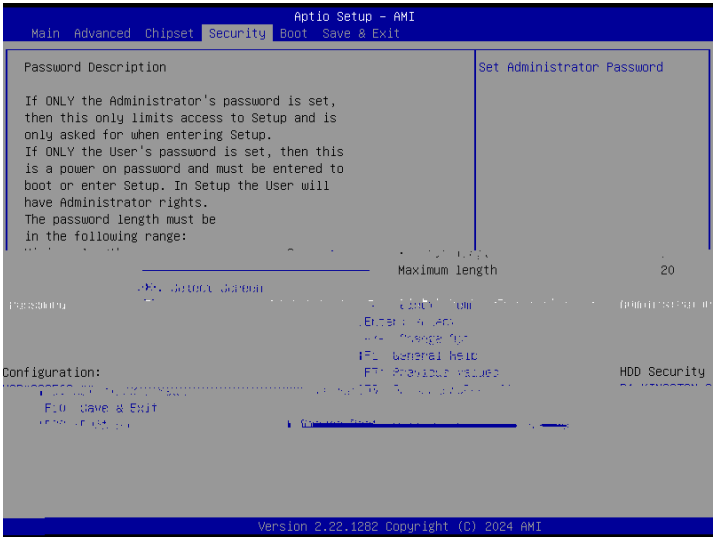
SATA Con f guration

SATA G

Onboard LAN Con f guration

G

7.7 Security



Administrator Password

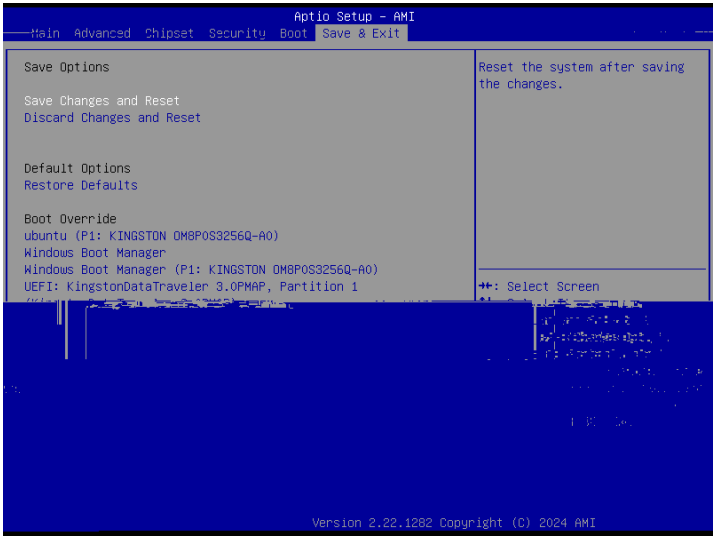
h ч

1. Administrator Password h <Enter> G
2. d Create New Password d 3~20 h

<Enter> h d Con f rm Password d h G

d Invalid Password! d h h G

7.9 Save&Exit



Save Changes and Reset

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Discard Changes and Reset

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Restore Defaults

G

8

8.1 DO/DI

JEC-1303LG DO/DI ч

(1) DO Pin2/Pin4/Pin6/Pin8/Pin10/Pin12/Pin14/Pin16 DO0~DO7 h
SIO GP65/GP86/GP63/GP64/GP40/GP41/GP42/GP43Ц

(2) DI Pin3~Pin10 DI0~DI7 h SIO
GP30/GP31/GP32/GP33/GP34/GP35/GP36/GP37Ц

(3) GPIO Group GP3x/4x/6x Logical Device 7Ц
GPIO Group GP8x Logical Device 9

(4) GP3x(30~37) Logical Device 7 CR 0xED Bit0~Bit7Ц
GP4x(40~43) Logical Device 7 CR 0xF1 Bit0~Bit3Ц
GP6x(63~65) Logical Device 7 CR 0xF9 Bit3~Bit5Ц
GP86 Logical Device 9 CR 0xF1 Bit6

(5) DO Pin3 GP65 / DI

```
#define SuperIo_Index_Port  0x2E
#define SuperIo_Data_Port   0x2F
#define GPIO_LDN7_DEVICE    0x07
#define GPIO_LDN9_DEVICE    0x09
#define GPIO_GROUP_3_IO_REGISTER    0xEC
#define GPIO_GROUP_3_DATA_REGISTER  0xED
#define GPIO_GROUP_4_IO_REGISTER    0xF0
#define GPIO_GROUP_4_DATA_REGISTER  0xF1
#define GPIO_GROUP_6_IO_REGISTER    0xF8
#define GPIO_GROUP_6_DATA_REGISTER  0xF9
#define GPIO_GROUP_8_IO_REGISTER    0xF0
#define GPIO_GROUP_8_DATA_REGISTER  0xF1
```

DO Pin3 GP65 / ч

```
//a.      Super IO  Configuration Mode
IoWrite8(SuperIo_Index_Port, 0x87);
IoWrite8(SuperIo_Index_Port, 0x87);
//b.                GPIO, LDN 7
IoWrite8(SuperIo_Index_Port, 0x07);
IoWrite8(SuperIo_Data_Port, GPIO_LDN7_DEVICE);
//c.      GP65      /
UINT8 Data8Ц
IoWrite8(SuperIo_Index_Port, GPIO_GROUP_6_DATA_REGISTER);
Data8 = IoRead8(SuperIo_Data_Port); //          GPIO Group 6
Data8 |= (0x1 << 5); //       bit        1  h       GPIO
//Data8 &=~(0x1 << 5);//       bit       0 h       GPIO
IoWrite8(SuperIo_Data_Port, Data8); //
//d.      Super IO  Configuration Mode
IoWrite8(SuperIo_Index_Port, 0xAA); //      Super IO Configuration Mode    h SuperIO
                                ,                Configuration Mode ь
```

```
    DI
//a.      Super IO   Conf guration Mode
loWrite8(Superlo_Index_Port, 0x87);
loWrite8(Superlo_Index_Port, 0x87);
//b.                GPIO, LDN 7
loWrite8(Superlo_Index_Port, 0x07);
loWrite8(Superlo_Data_Port, GPIO_LDN7_DEVICE);
//c.      GPIO Group 3          GP33
UINT8 BitO fset = 3;
UINT8 Data8 H

loWrite8(Superlo_Index_Port, GPIO_GROUP_3_DATA_REGISTER);
Data8 = loRead8(Superlo_Data_Port);
Data8 = Data8 >> BitO fset;
Data8 = Data8 & 0x1;
if (Data8){
return 1;//      GPIO
}else{
 return 0;//      GPIO
}
//d.      Super IO   Conf guration Mode
loWrite8(Superlo_Index_Port, 0xAA); //      Super IO Conf guration Mode    h SuperIO
                                ,                Conf guration Mode
```

8.2 WDT

```
#def ne Superlo_Index_Port 0x2E
#def ne Superlo_Data_Port 0x2F
#def ne GPIO_LDN8_DEVICE 0x08
UINT8 Data8 H
//a.      Super IO   Conf guration Mode
loWrite8(Superlo_Index_Port, 0x87);
loWrite8(Superlo_Index_Port, 0x87);
//b.                GPIO, LDN 8
loWrite8(Superlo_Index_Port, 0x07);
loWrite8(Superlo_Data_Port, GPIO_LDN8_DEVICE);
//c. Enabled WDT
loWrite8(Superlo_Index_Port, 0x30);
loWrite8(Superlo_Data_Port, loRead8(Superlo_Data_Port) | 0x01);
//Disable WDT
//loWrite8(Superlo_Index_Port, 0x30);
//loWrite8(Superlo_Data_Port, loRead8(Superlo_Data_Port) & 0xFE);
//d.      WDT                    Register 0xF0   Bit3        1                0
loWrite8(Superlo_Index_Port, 0xF0);
//
loWrite8(Superlo_Data_Port, loRead8(Superlo_Data_Port) | 0x08);
//
// loWrite8(Superlo_Data_Port, loRead8(Superlo_Data_Port) & 0xF7);
//loWrite8(Superlo_Data_Port, 0x0);
```

```
//e.      WDT                5    /
loWrite8(Superlo_Index_Port, 0xF1);
loWrite8(Superlo_Data_Port, 0x5);
//       WDT
//loWrite8(Superlo_Index_Port, 0xF1);
//f.      Super IO   Con f guration Mode
loWrite8(Superlo_Index_Port, 0xAA); //       Super lO Con f guration Mode     h SuperlO
                                    ,                  Con f guration Mode G
```

9

h G
h h
h G

10

10.1

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		1Hט 2Hט 12
	⊄ d	
		G h
		1Hט 2Hט 3Hט h
		ÿ ÿ Hט
		ÿ Winpe ÿ h h
IHO h		PCI ISA Hט Hט h
	BIOS	h BIOS Setup h BIOS Setup
BIOS h		
Boot device not found	BIOS h h	BIOS ⊄ d (Boot) h
USB	USB 2.0 h USB 2.0	USB 2.0
	USB	1Hט USB Legacy Support ÿ USB ÿ 2Hט h USB