Version

G

G

G

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1

1.1

JET-5310 BOX Intel Tiger Lake U
G Hυ
Hυ G G
INTEL TGU i3Hυi5Hυi7 CPU HDMI+DP
3 1G 1 4GHυ5G G LPC
G
WINDOWS LINUX G

1.2

	- JET-5310
	- BOX

2

2.1

2.2

2.3

2.3.1

-
-
-
-
-

2.4

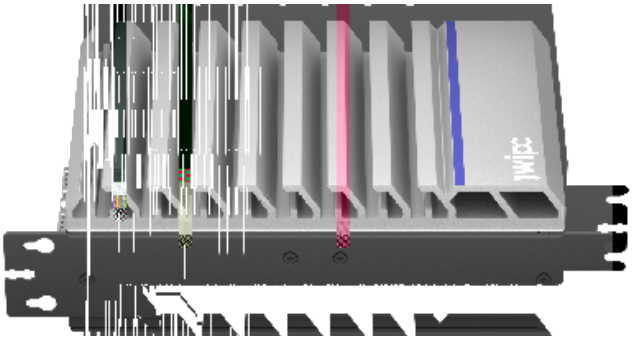
-
-
-
- 50mm 100mm
- (
-
- I/O 0.5V

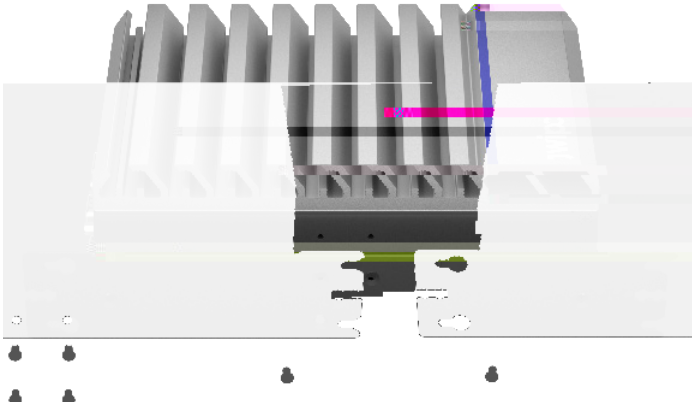
3

3.1

3.3 JET-5310

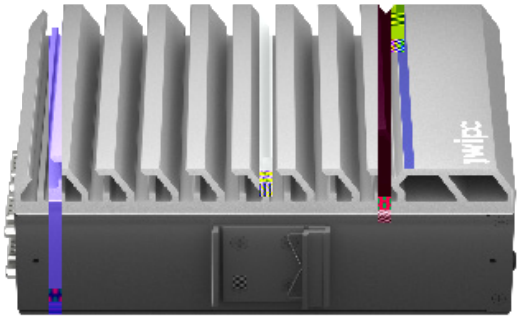
˜ 2 , M3 x 5.6 G





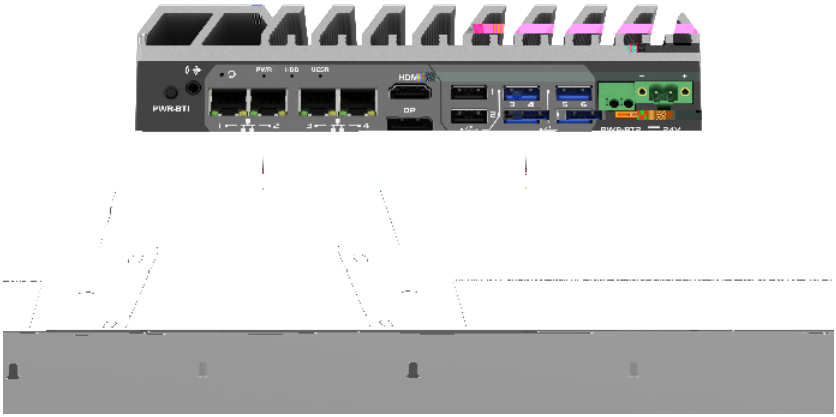
3.4 JET-5310

˜ 2 , M3 x 5.6 G



3.5 JET-5310

˜ 2 , M3 x 5.6 G



4

4.1

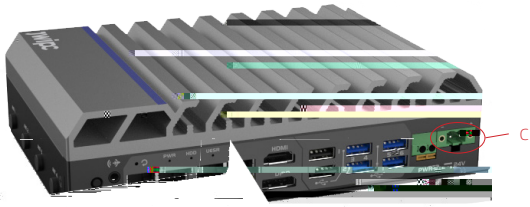
⚠
G

⚠
G G

⚠
G

G I/O USB G I/O G

4.2

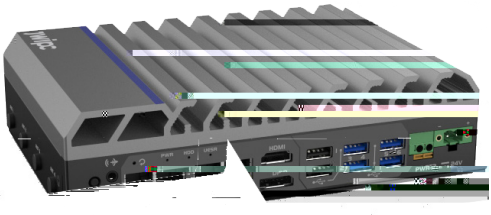
DCIN +12V~36V G	

⚠
G

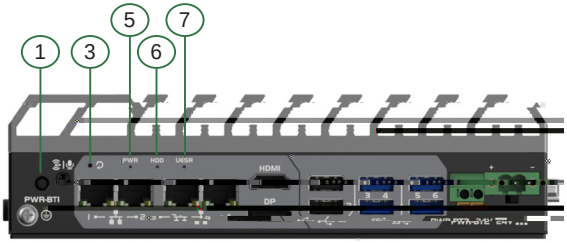
G

5

5.1



5.2 IO



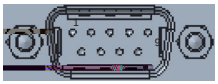
1. PWR_BTN1
2. AUDIO Hυ
3. RECOVER
4. LAN1/2/3/4 RJ45
5. PWR
6. HDD
7. USER: Battery Low
8. HDMI HDMI
9. DP DP
10. USB2.0 USB2.0 Type-A
11. USB3.0 USB3.2 Gen2 Type-A
12. PWR_BTN2
13. DC_IN DC
14. GPIO 3pin I²C +3pin CANBus 2.0 +8pin GPIO
15. COM1/2/3/4
16. ANT1/2/3/4 WIFI

5.3

		LED	
PWR	PC		DC
			PC
HDD			SATA
			NVME

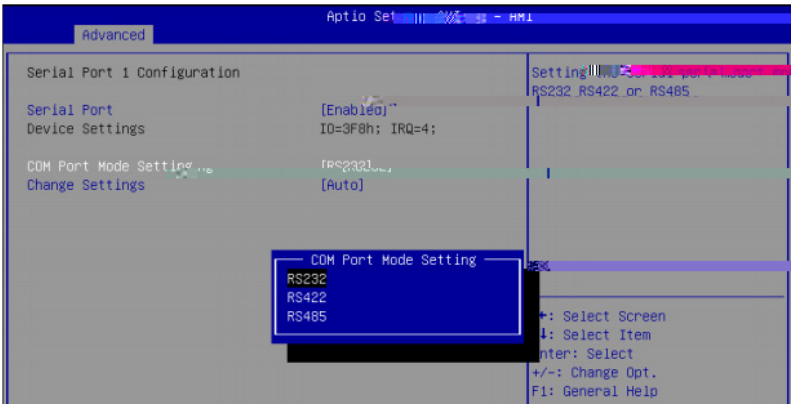
5.4 DCIN1

5.5 COM1/2/3/4



PIN	RS232	RS422	RS485
1	DCD	422TX-	485-
2	SIN	422TX+	485+
3	SOUT	422RX+	/
4	DTR	422RX-	/
5	GND	/	/
6	DSR	/	/
7	RTS	/	/
8	CTS	/	/
9	RI	/	/

COM1-4 RS232/422/485 BIOS

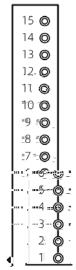


5.6

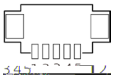
5.6.1 COM5/6

	1	NDCD	2	NSIN
	3	NSOUT	4	NDTR
	5	GND	6	NDSR
	7	NRTS	8	NCTS
	9	NRI	10	GND

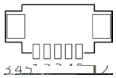
5.6.2 PH1

	1	GND	2	GP_71
	3	GP_70	4	GP_87
	5	GP_86	6	GP_85
	7	GP_84	8	GP_83
	9	GP_82	10	GPIO_PWR
	11	CAN1H	12	CAN1L
	13	GND	14	I2C0_SCL_S
	15	I2C0_SDA_S		

5.6.3 F_PANEL

	1	VCC3
	2	SATA_SSD_LED#
	3	PCH_SATA_LED_N_R
	4	GND
	5	SATA_LED+

5.6.4 INVT1

	1	GND
	2	PWM_OUT1
	3	BKL_EN
	4	BKL_PWR

5.6.6 USB

	1	GND
	2	USB_P9_DP
	3	USB_P9_DN
	4	VCC5

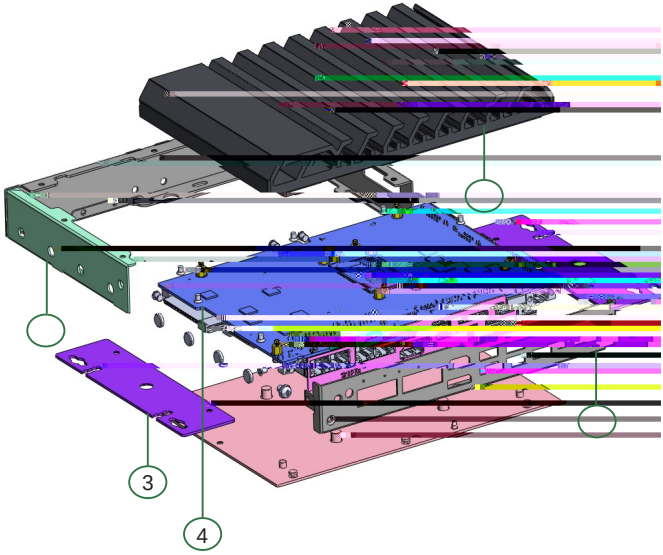
5.6.8 JLVDS1

5.6.9 LVDS

	1	LCD_VCC	2	LCD_VCC
	3	LCD_VCC	4	GND
	5	GND	6	GND
	7	DATA0N	8	DATA0P
	9	DATA1N	10	DATA1P
	11	DATA2N	12	DATA2P
	13	GND	14	GND
	15	CLK1_RN	16	CLK1_RP
	17	DATA3N	18	DATA3P
	19	DATA4N	20	DATA4P
	21	DATA5N	22	DATA5P
	23	DATA6N	24	DATA6P
	25	GND	26	GND
	27	CLK2_RN	28	CLK2_RP
	29	DATA7N	30	DATA7P

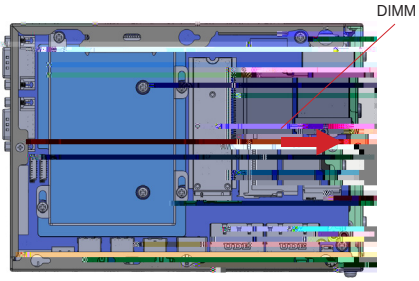
6

6.1 JET-5310



1		2		3	
4		5	M3X5_	6	M3X5_
7		8	6#32X5	9	

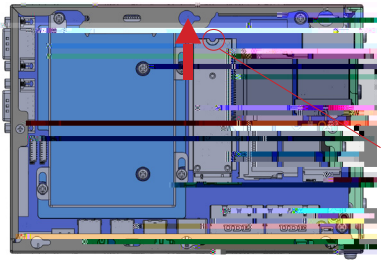
6.2



DIMM G

1.
2.
3. DIMM
4. DIMM 30° G

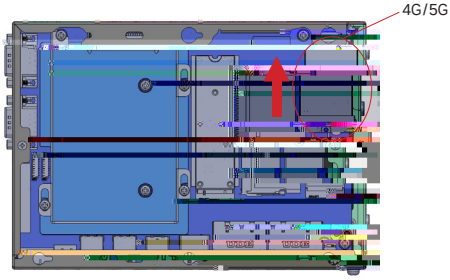
6.3 M.2 2242/2280



M.2 1 M2 M.2 2242/2280 SATA SSD G

1. 30°
2. M.2 2242 M.2 2280 M.2 2242 G

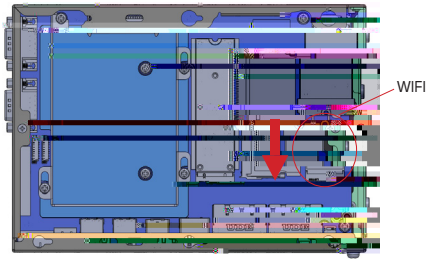
6.4 4G/5G



4G/5G G

4G/5G 30° G

6.5 WIFI



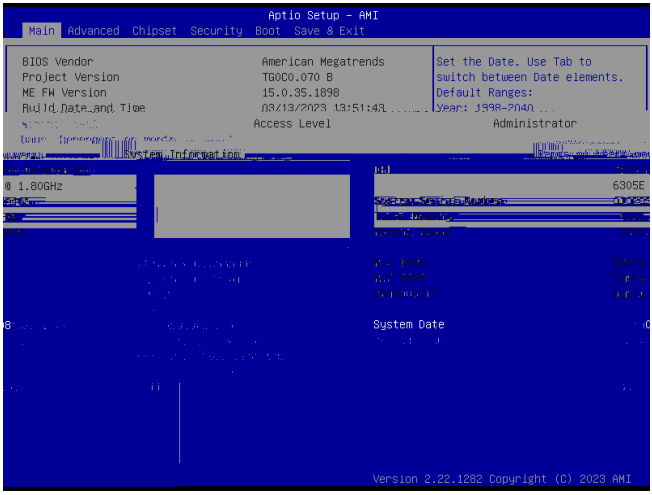
WIFI G

WIFI 30° G

7.3 BIOS

Main		BIOS
Advanced		BIOS
Chipset		
Security		
Boot		
Save & Exit		BIOS

7.4 Main



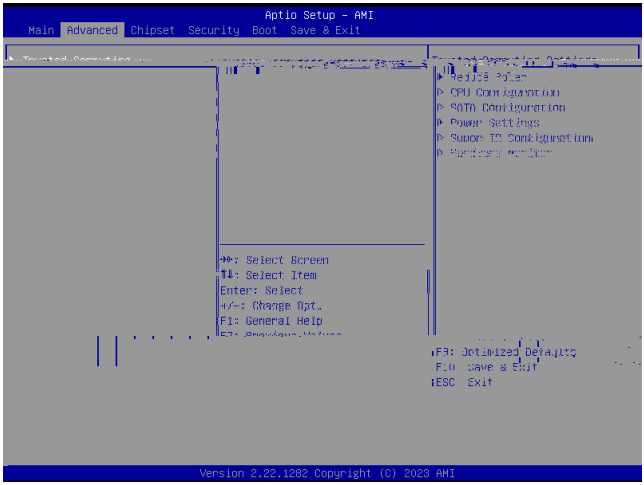
System Date ( )

, “ , / / ” G

System Time

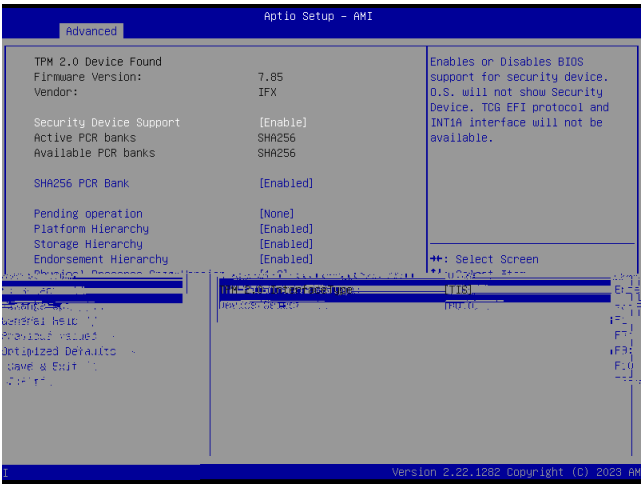
< >< >< > G

7.5 Advanced



Trusted Computing		
Reduce Power		
CPU Configuration	CPU	
SATA Configuration	SATA	
Power Settings		
Super IO Configuration		
Hardware Monitor		

- Trusted Computing <Enter> G



Security Device Support

G Disabled,Enabled.

SHA256 PCR Bank

SHA256 PCR Bank G Disabled,Enabled.

Pending operation

G None,TPM Clear.

Platform Hierarchy

G Disabled,Enabled.

Storage Hierarchy

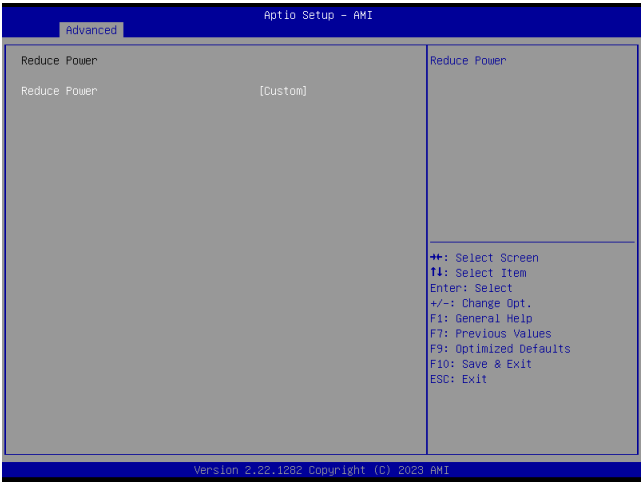
G Disabled,Enabled.

Endorsement Hierarchy

G Disabled,Enabled.

Physical Presence Spec Version

- Reduce Power <Enter> G



Reduce Power

G Custom,Disabled,Enabled.

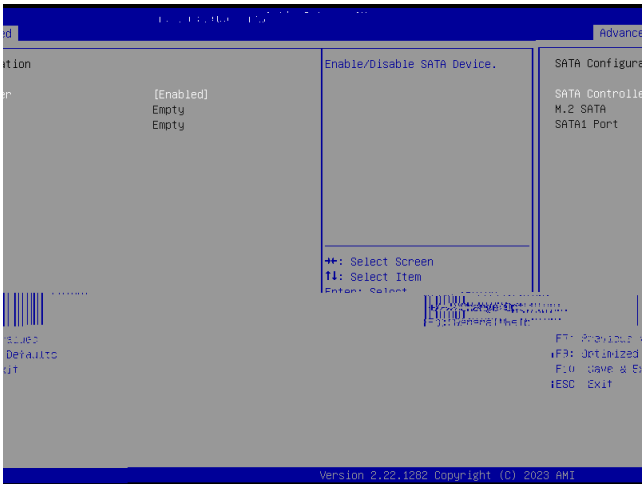
- CPU Conf guration <Enter> G



Turbo Mode

Turbo G Disabled,Enabled.

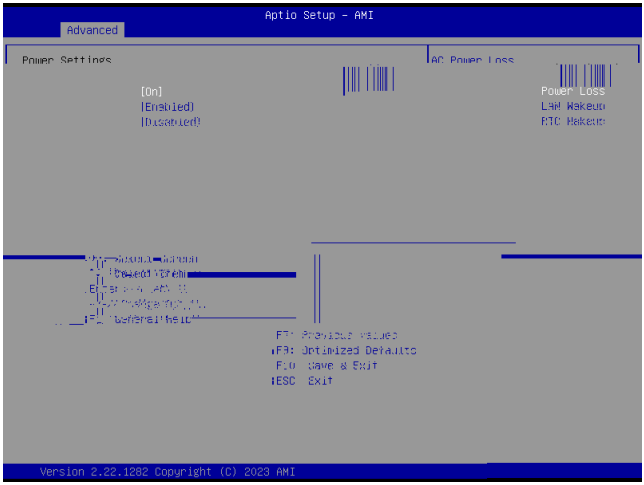
- SATA Conf guration <Enter> G



SATA Controller

SATA G Disabled,Enabled.

- Power Settings <Enter> G



Power Loss

“ ” G On,O f ,Last State.

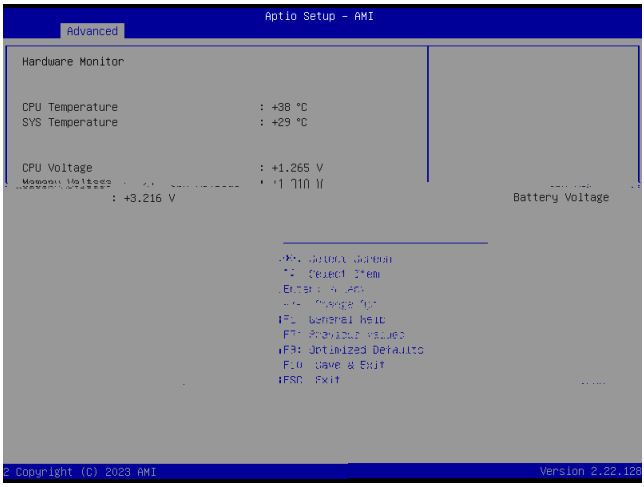
LAN Wakeup

G Disabled,Enabled.

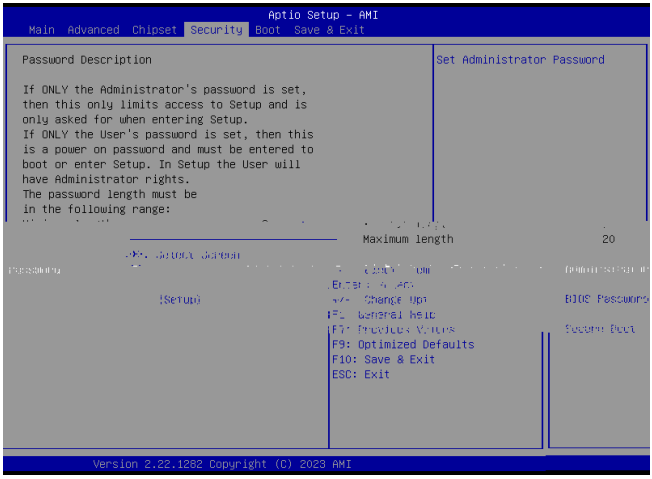
RTC Wakeup

G Disabled,Enabled.

- Hardware Monitor <Enter> G



7.7 Security



Administrator Password

1. Administrator Password <Enter> G

2. “ Create New Password ” 3~20

<Enter> “ Confrm Password ” G

“ Invalid Password! ” G

“ Administrator Password ” “ Enter Current Password ”

“ Create New Password ” <Enter> G

BIOS Password

G Setup&Post,Setup.

7.8 Boot



Setup Prompt Timeout

G

Boot NumLock State

NumLock G On,Of.

Full Screen Logo

G Disable,Enable.

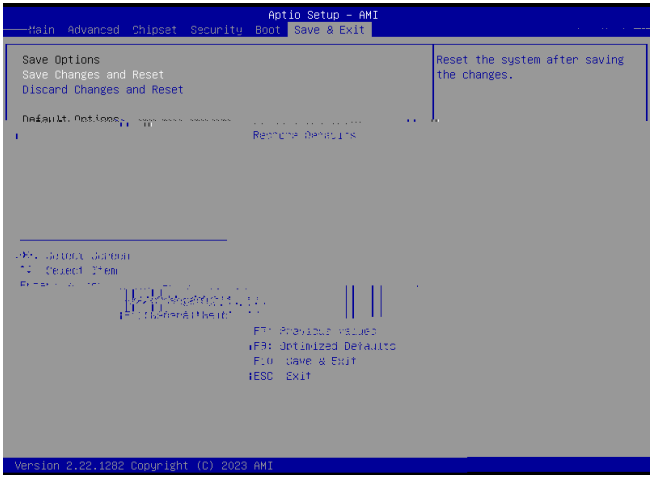
USB Mass Storage Driver Suoport

USB G Disable,Enable.

Boot Option #1/2/3/4/5/6/7

1 G NVME,Hard Disk:UEFI OS (P0: NS512GSSD340-I),USB Hard Disk,USB Key,USB CD/DVD,Network,UEFI AP: UEFI: Built-in EFI Shell.

7.9 Save&Exit



Save Changes and Reset

G

Discard Changes and Reset

G

Restore Defaults

G

8

JET-1501 JEC-5310 GPIO&Watch Dog

```
    unsigned charret;

    ret = iopl(3);

    if (ret)

    {

        printf("ret = %d \n", ret);

        printf("errno = %d \n", errno);

        printf("error for iopl \n");

        return 1;

    }

    outb(Data, GpioAddress);

    return 0;

}
```

8.2 GPIO

```
        GPIO1~GPIO8     Super IO
GPIO1 --> SIO GPIO71
GPIO2 --> SIO GPIO70
GPIO3 --> SIO GPIO87
GPIO4 --> SIO GPIO86
GPIO5 --> SIO GPIO85
GPIO6 --> SIO GPIO84
GPIO7 --> SIO GPIO83
GPIO8 --> SIO GPIO82

ITE8786 GPIO          Hט
#define ITE8786_Index_Port      0x2E
#define ITE8786_Data_Port       0x2F
#define GPIO_LDN_DEVICE                 0x07
#define GPIO_BASE_ADDRESS               0xa00
GPIO Group 7
#define GPIO7_INPUT_OUTPUT_REGISTER     0xce
#define GPIO7_DATA_REGISTER             GPIO_BASE_ADDRESS
+ 0x06
GPIO Group 8
#define GPIO8_INPUT_OUTPUT_REGISTER     0xcf
#define GPIO8_DATA_REGISTER             GPIO_BASE_ADDRESS
+ 0x07
```

```
//a.        Super IO      Configuration Mode
IoWrite8(ITE8786_Index_Port, 0x87);
IoWrite8(ITE8786_Index_Port, 0x01);
IoWrite8(ITE8786_Index_Port, 0x55);
IoWrite8(ITE8786_Index_Port, 0x55);

//b.                    GPIO, LDN 7
IoWrite8(ITE8786_Index_Port,0x07);
IoWrite8(ITE8786_Data_Port,GPIO_LDN_DEVICE);

   Super IO GPIO Group 7
//c.        GPIO Group7      70~77         GPI
UINT8 BitOffset;
UINT8 GpioNumber;
//Offset 0xce, bits 0~7                0    GPIO70~77         GPI                  G    //              GPIO
                    GPI     GPO                    GPIO          GPIO72                        GPI
   GPO                GPI        GPO G
for(GpioNumber=0x70; GpioNumber<=0x77; GpioNumber++)
{
    BitOffset = GpioNumber - 0x70;
    IoWrite8(ITE8786_Index_Port,GPIO7_INPUT_OUTPUT_REGISTER);
    Data8 = IoRead8(ITE8786_Data_Port);
    Data8 = Data8&(~(0x1<<BitOffset));
    IoWrite8(ITE8786_Data_Port,Data8);
}

//        GPIO Group7      70~77         GPO                                    //    G Offset 0xce, bits
0~7                1    GPIO70~77         GPO                  G
for(GpioNumber=0x70; GpioNumber<=0x77; GpioNumber++)
{
    BitOffset =GpioNumber - 0x70;
    IoWrite8(ITE8786_Index_Port,GPIO7_INPUT_OUTPUT_REGISTER);
    Data8 = IoRead8(ITE8786_Data_Port);
    Data8 = Data8|(0x1<<BitOffset);
    IoWrite8(ITE8786_Data_Port,Data8);
}

//d.    GPIO       G                  GPO              GPIO              GPI              G
//GPIO7_DATA_REGISTER    bits0~7              GPIO70~77              G          bit              0
          GPIO                    1              G
for(GpioNumber=0x70; GpioNumber<=0x77; GpioNumber++)
{
    BitOffset = GpioNumber - 0x70;
    Data8 = IoRead8(GPIO7_DATA_REGISTER);
    Data8 &=~(0x1<<BitOffset);//        bit        0          GPIO
    //Data8 |= 0x1<<BitOffset; /*        bit          1          GPIO              */
    IoWrite8(GPIO7_DATA_REGISTER,Data8);
}

//e.              GPIO                  GPIO7_DATA_REGISTER    bits0~7
GPIO70~77                G
```

```
For(GpioNumber=0x70; GpioNumber<=0x77; GpioNumber++)
{
    BitOffset = GpioNumber - 0x70;
    Data8 = IoRead8(GPIO7_DATA_REGISTER);
    Data8 = Data8>>BitOffset;
    Data8 = Data8 &0x1;
}
if(Data8&0x1){
        return 1;//      GPIO
    }else{
        return 0;//      GPIO
}

  Super IO GPIO Group8
//c-1.      GPIO Group8    80~87      GPI                                    G
UINT8 BitOffset;
UINT8 GpioNumber;
// IN_OUT_SEL_REG_GP8 bits 0~7              0   GPIO80~87      GPI          //      G
  GPIO                    GPI    GPO              //GPIO        GPIO82
  GPI            GPO            GPI      GPO G
for(GpioNumber=0x80; GpioNumber<=0x87; GpioNumber++)
{
    BitOffset = GpioNumber - 0x80;
    IoWrite8(ITE8786_Index_Port, GPIO8_INPUT_OUTPUT_REGISTER);
    Data8 = IoRead8(ITE8786_Data_Port);
    //GPIO80~87      Data8      Bit0~Bit7      Bit                  GPIO    //          G
    Data8 = Data8&(~(0x1<<BitOffset));
    IoWrite8(ITE8786_Index_Port, GPIO8_INPUT_OUTPUT_REGISTER);

    IoWrite8(ITE8786_Data_Port,Data8);
}

//      GPIO Group8    80~87      GPO                                  //    G IN_OUT_SEL_
REG_GP8 bits 0~7            1   GPIO80~87      GPO      //          G
for(GpioNumber=0x80; GpioNumber<=0x87; GpioNumber++)
{
    BitOffset =GpioNumber - 0x80;
    IoWrite8(ITE8786_Index_Port, GPIO8_INPUT_OUTPUT_REGISTER);
    Data8 = IoRead8(ITE8786_Data_Port);
    //GPIO80~87      Data8      Bit0~Bit7      Bit      1          GPIO    //          G
    Data8 = Data8|(0x1<<BitOffset);
    IoWrite8(ITE8786_Index_Port, GPIO8_INPUT_OUTPUT_REGISTER);
    IoWrite8(ITE8786_Data_Port,Data8);
}

//d-1.    GPIO      G                GPO          GPIO          GPI
          G
// IN_OUT_DATA_REG_GP8   bits0~7          GPIO80~87          G
  bit          0          GPIO                  1          G
for(GpioNumber=0x80; GpioNumber<=0x87; GpioNumber++)
{
    BitOffset = GpioNumber - 0x80;
```

```
    //                          GPIO
    // " IN_OUT_DATA_REG_GP8 "              Data O f set Register      G
    Data8 = IoRead8(GPIO_BASE_ADDRESS + IN_OUT_DATA_REG_GP8);
    Data8 &=~(0x1<<BitO f set); //      bit      0        GPIO
    //Data8 |= 0x1<<BitO f set; /*      bit      1        GPIO              */
    IoWrite8(GPIO_BASE_ADDRESS + IN_OUT_DATA_REG_GP8,Data8);
}

//e-1.          GPIO                IN_OUT_DATA_REG_GP8   bits0~7          GPIO80~87
      G
For(GpioNumber=0x80; GpioNumber<=0x87; GpioNumber++)
{
    BitO f set = GpioNumber - 0x80;
    Data8 = IoRead8(GPIO_BASE_ADDRESS + IN_OUT_DATA_REG_GP8);
    Data8 = Data8>>BitO f set;
    Data8 = Data8 &0x1;
}
if(Data8&0x1){
          return 1; //      GPIO
      }else{
          return 0; //      GPIO
}

//f.       Super IO    Con f guration Mode
IoWrite8(ITE8786_Index_Port, 0x02);
IoWrite8(ITE8786_Index_Port, 0x02); //      Super IO Con f guration Mode      SuperIO
                          ,                Con f guration Mode G
```

8.3 Watch Dog

8.3.1 Watch Dog

```
//b.                    GPIO, LDN 7,      GP10       WDT
IoWrite8(SuperIO_Index_Port, 0x07);
IoWrite8(SuperIO_Data_Port , WDT_LDN_DEVICE);

IoWrite8(SuperIO_Index_Port, 0x25);
IoWrite8(SuperIO_Data_Port , (IoRead8(SuperIO_Data_Port) | 0x01));

IoWrite8(SuperIO_Index_Port, 0xC0);
IoWrite8(SuperIO_Data_Port , (IoRead8(SuperIO_Data_Port) | 0x01));

IoWrite8(SuperIO_Index_Port, 0xC8);
IoWrite8(SuperIO_Data_Port , (IoRead8(SuperIO_Data_Port) | 0x01));

IoWrite8(SuperIO_Index_Port, 0xF1);
IoWrite8(SuperIO_Data_Port , (IoRead8(SuperIO_Data_Port) |0x44));

IoWrite8(SuperIO_Index_Port, 0xF4);
IoWrite8(SuperIO_Data_Port , (IoRead8(SuperIO_Data_Port) |0x08));

//c. Clear WDT
IoWrite8(SuperIO_Index_Port, 0x71);
IoWrite8(SuperIO_Data_Port , ((IoRead8(SuperIO_Data_Port) & ~0x10) | 0x01));

//d.       WDT
IoWrite8(SuperIO_Index_Port, 0x72);
Data8 = IoRead8(SuperIO_Data_Port );
Data8 = (Data8&0xc0)|0xc0; //WDT
// Data8 = (Data8&0x40)|0x40; /*WDT                    */
IoWrite8(SuperIO_Data_Port, Data8 );

 //e.       WDT   WDT          0~255          0      WDT                    0          WDT
                                        G
UINT8 Timer;
IoWrite8(SuperIO_Index_Port,0x73);
IoWrite8(SuperIO_Data_Port,Timer); //          Timer                1    255              G
IoWrite8(SuperIO_Index_Port,0x74);
 IoWrite8(SuperIO_Data_Port,0x00); //          Timer              0x00                    Timer
                G

//f.       WDT
IoWrite8(SuperIO_Index_Port,0x73);
IoWrite8(SuperIO_Data_Por, 0x00);

//g.                    WDT Timer
IoWrite8(SuperIO_Index_Port,0x73);
IoWrite8(SuperIO_Data_Port,Timer); //Timer                    1    255              G

//h.       Super IO     Configuration Mode
IoWrite8(SuperIO_Index_Port, 0x02);
IoWrite8(SuperIO_Index_Port, 0x02);//       Super IO Configuration Mode
//SuperIO                                    ,              Configuration Mode G
```

9

9.1

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