

Vhuvlrq 1.0

1

1.1

JMC-7310 I/O
LAN, COM, DP/HDMI 2nd,
, PCIe PCI

JMC-7311	1	1 x PCIex16
JMC-7312	2	2 x PCI/1 x PCIex16+1 x PCI/1 x PCIex16+1 x PCIex4
JMC-7313	3	1 x PCIex16+2 x PCI
JMC-7314	4	1 x PCIex16+2 x PCI+1 x PCIex4

1.2

	- JMC-7310	- JMC-7311	- JMC-7312	- JMC-7313	- JMC-7314
CPU	- LGA1200 Gen 10th/11th Core™i3/i5/i7/i9 Pentium®/Celeron®/ ® Processor				
	- W480E/H420E(JMC-7314 W480E)				
	- 2 x260-Pin DDR4 SODIMM, DDR4 2933/2666 MHz 64GB (W480E SKU support ECC)				
	- HDMI 2nd/DP/DVI - 1xVGA, VGA 1920*1200@60Hz - 1xHDMI,HDMI 4096*2160@24Hz				
	- 1 x 2.5 " HDD/SSD(2) W480E SATA RAID 0/1, - 1 x mSATA				
	- Line-out, Mic-in				
	- 2 , LAN1: I219LM, LAN2: I210AT				
USB	- W480E:2 x USB3.2(Gen2), 6 x USB3.2(Gen1), 2 x USB2.0(Internal), 1 x USB dongle - H420E:6 x USB3.2(Gen1), 2 x USB2.0, 1 x USB2.0(Internal)				
	- 6 COM 2x RS232/RS422/RS485, 4 x RS-232 ( )				
PS2	- 1 (, PS/2 KB/Mouse)				
TPM	-				
	- 1				
	- 2, 1x Power LED , 1x HDD LED				
	- DC IN 9~36V				

	- W480E 2x Mini-PCIe (SIM , 4G 1 mSATA) - H420E 1x Mini-PCIe (SIM , 4G), 1x mSATA JMC-7311 1 x PCIex16 JMC-7312 2 x PCI/1 x PCIex16+1 x PCI/1 x PCIex16+1 x PCIex4 JMC-7313 1 x PCIex16+2 x PCI JMC-7314 1 x PCIex16+2 x PCI+1 x PCIex4
	- / 65W -10 ~50 , 35W -10 ~60 ;95%@40 - / -40 ~85 95%@40
	- With SSD: 2 Grms @ 5 ~ 500 Hz, random, 1 hr/axis - With 2.5" HDD: 1 Grms @ 5 ~ 500 Hz, random, 1 hr/axis
	- 255 /
BIOS	- AMI UEFI BIOS
	- Windows 10(64 bit), Linux OS, Ubuntu 20.04
(W{D{H)	- JMC-7310 230 (W) x 192 (D) x 88 (H) mm - JMC-7311 230 (W) x 192 (D) x 118 (H) mm - JMC-7312 230 (W) x 192 (D) x 138 (H) mm - JMC-7313 230 (W) x 192 (D) x 158 (H) mm - JMC-7314 230 (W) x 192 (D) x 178 (H) mm

3

3.1

□ 19″ ■ □
■ □ VESA □
□ _____

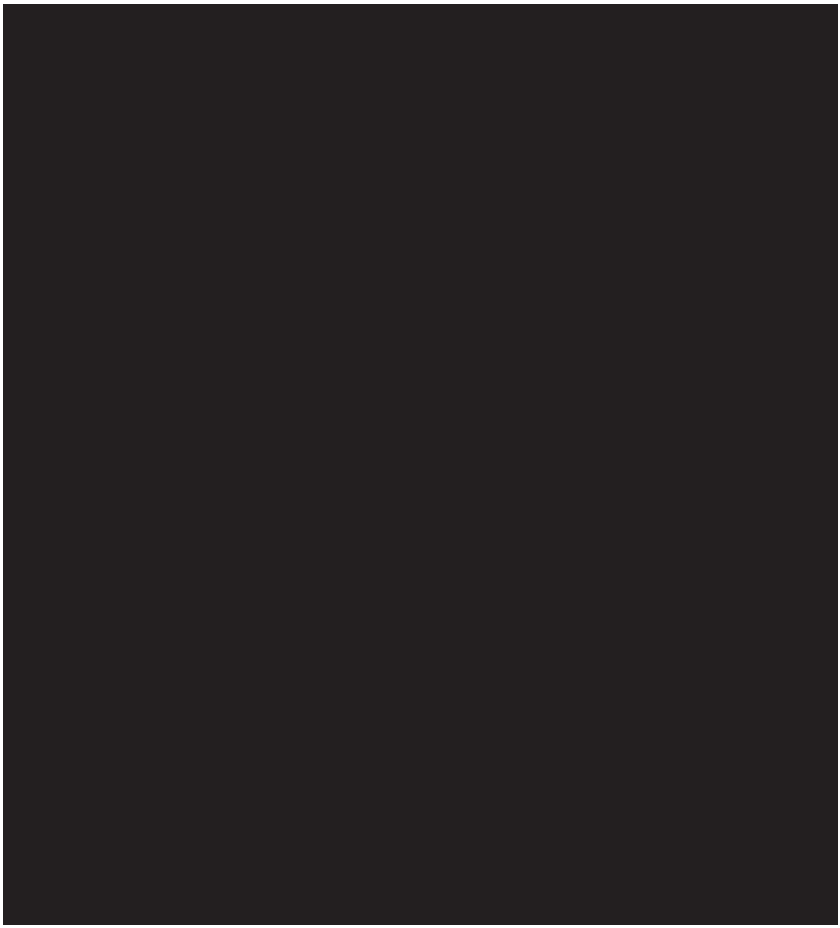
3.2 JMC-7310

mm



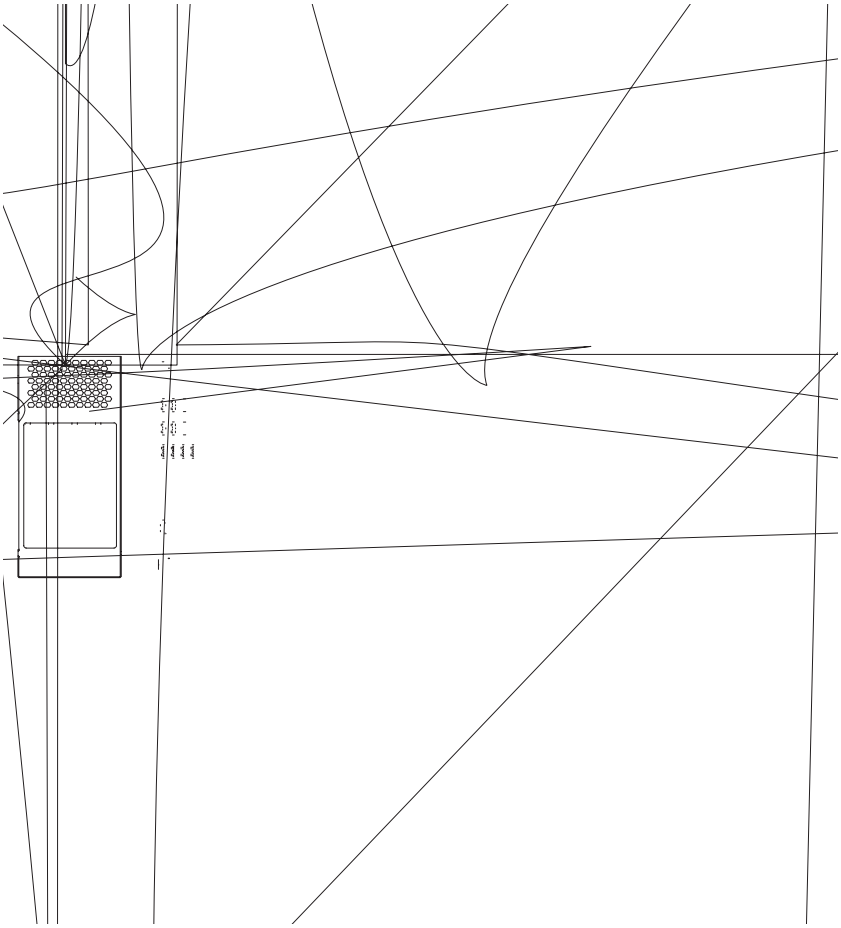
3.3 JMC-7311

mm



3.6 JMC-7314

mm



4

4.1

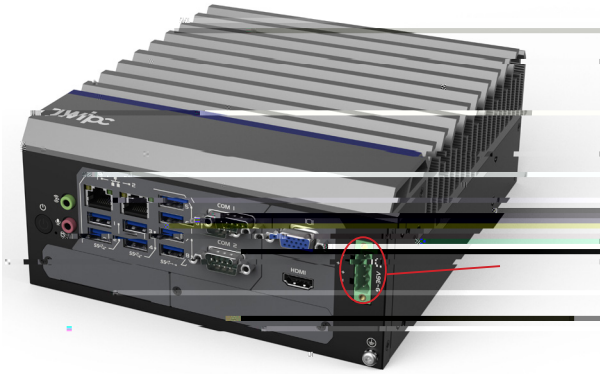
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I/O USB I/O

4.2

DCIN	

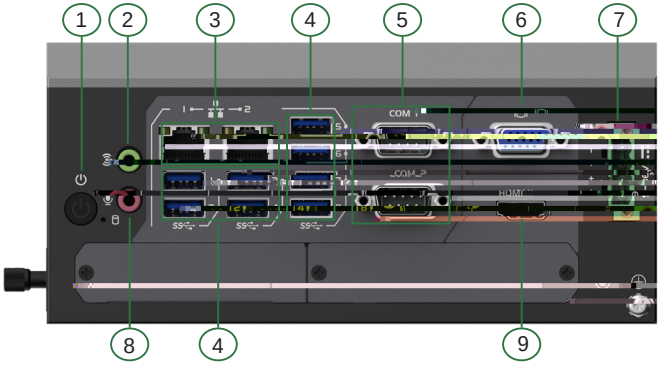
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5

5.1 JMC-7310

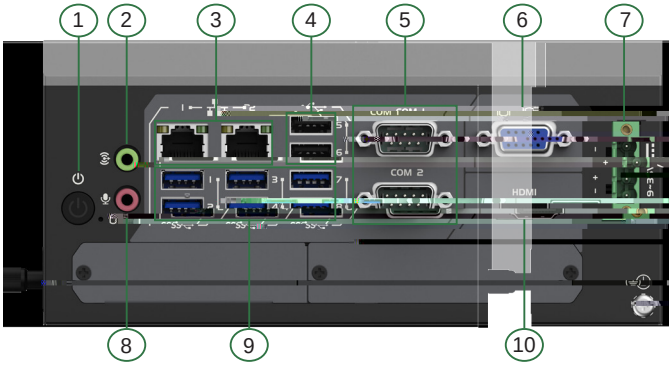


5.1.1 JMC-7310W IO



1.Power Button
2. Line out
3. LAN RJ45
4. USB3.0 USB3.0
5. COM COM
6. VGA VGA
7. DC_IN DC
8. Mic in
9. HDMI HDMI

5.1.2 JMC-7310H IO

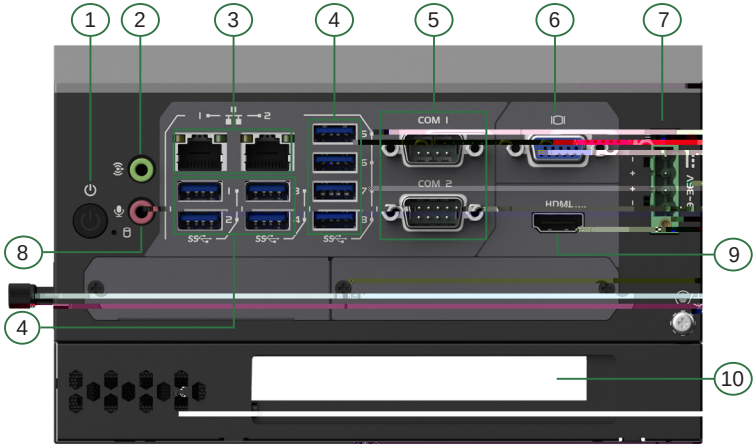


1.Power Button
2. Line out
3. LAN RJ45
4. USB2.0 USB2.0
5. COM COM
6. VGA VGA
7. DC_IN DC
8. Mic in
9. USB3.0 USB3.0
10. HDMI HDMI

5.2 JMC-7311

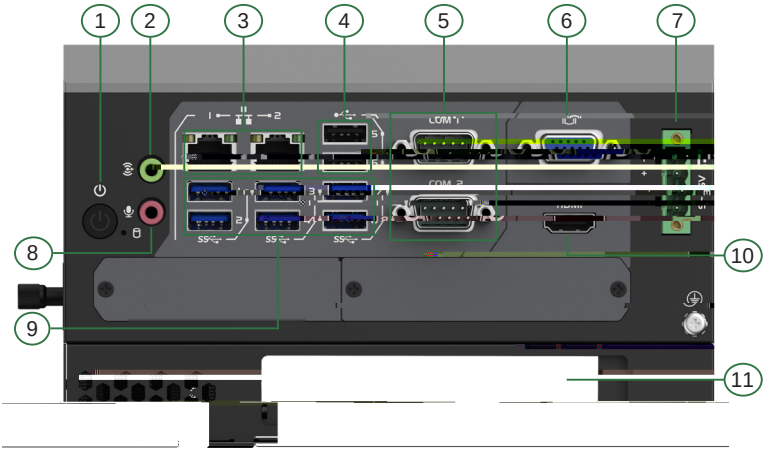


5.2.1 JMC-7311W IO



1.Power Button
2. Line out
3. LAN RJ45
4. USB3.0 USB3.0
5. COM COM
6. VGA VGA
7. DC_IN DC
8. Mic in
9. HDMI HDMI
10. JMC-7311 1 x PCIex16

5.2.2 JMC-7311H IO

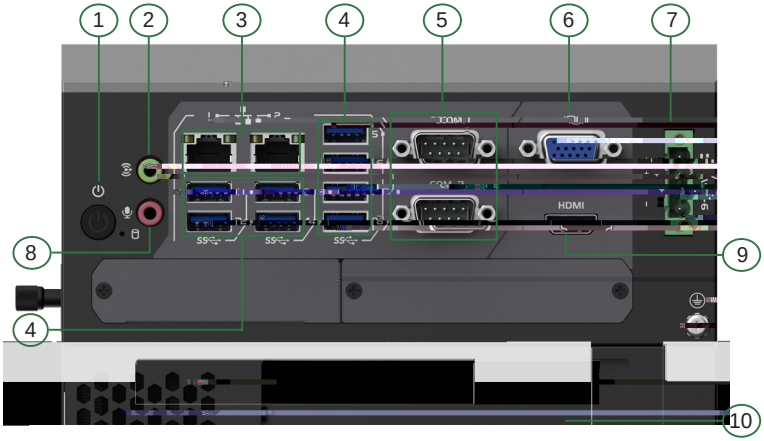


1.Power Button
2. Line out
3. LAN RJ45
4. USB2.0 USB2.0
5. COM COM
6. VGA VGA
7. DC_IN DC
8. Mic in
9. USB3.0 USB3.0
10. HDMI HDMI
11. JMC-7311 1 x PCIex16

5.3 JMC-7312

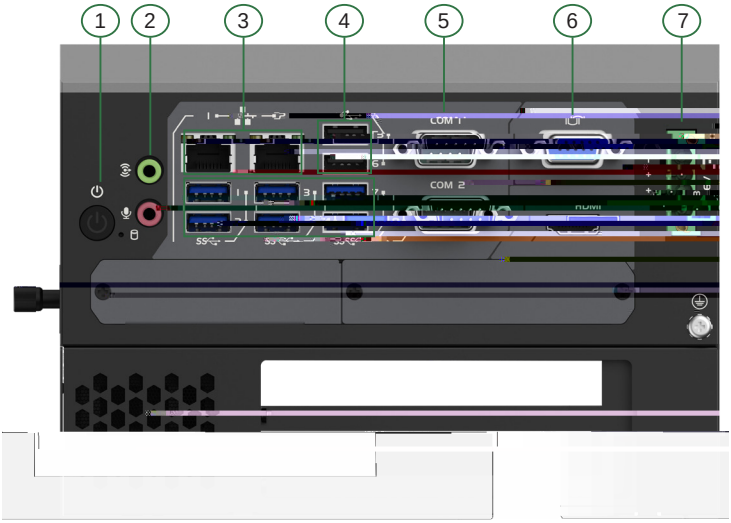


5.3.1 JMC-7312W IO



1.Power Button
2. Line out
3. LAN RJ45
4. USB3.0 USB3.0
5. COM COM
6. VGA VGA
7. DC_IN DC
8. Mic in
9. HDMI HDMI
10. JMC-7312 2 x PCI/1PCIex16+1 x PCI/1PCIex16+1 x PCIex4

5.3.2 JMC-7312H IO

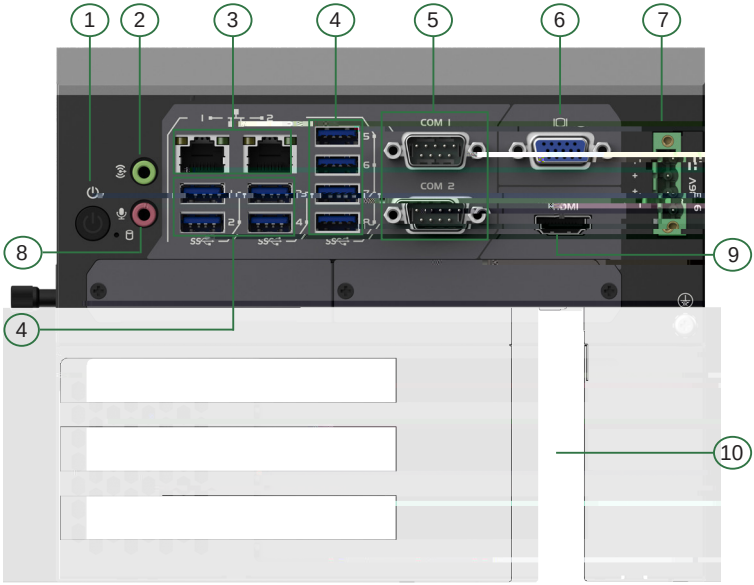


1.Power Button
2. Line out
3. LAN RJ45
4. USB2.0 USB2.0
5. COM COM
6. VGA VGA
7. DC_IN DC
8. Mic in
9. USB3.0 USB3.0
10. HDMI HDMI
11.

5.4 JMC-7313



5.4.1 JMC-7313W IO

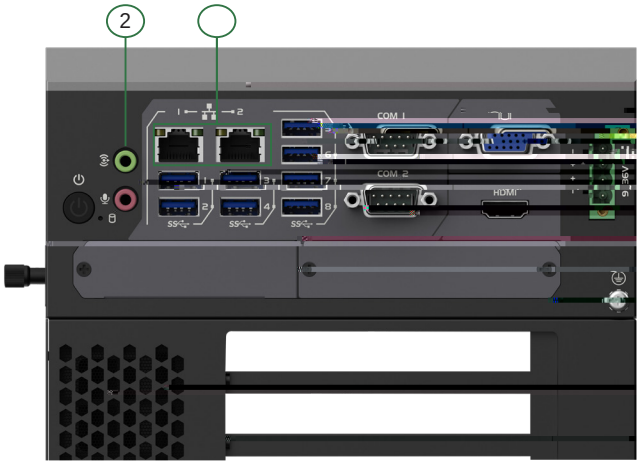


1.Power Button
2. Line out
3. LAN RJ45
4. USB3.0 USB3.0
5. COM COM
6. VGA VGA
7. DC_IN DC
8. Mic in
9. HDMI HDMI
10. JMC-7313 1 x PCIex16+2 x PCI

5.5 JMC-7314



5.5.1 JMC-7314W IO



1.Power Button
2. Line out
3. LAN RJ45
4. USB3.0 USB3.0
5. COM COM
6. VGA VGA
7. DC_IN DC
8. Mic in
9. HDMI HDMI
10. JMC-7314 1 x PCIex16+2 x PCI+1 x PCIex4

5.8

5.8.1 JDP1

	1	DP1_PWR	2	DP1_PWR
	3	GND	4	GND
	5	DDI2_TX0_DP	6	DDI2_TX2_DP
	7	DDI2_TX0_DN	8	DDI2_TX2_DN
	9	GND	10	GND
	11	DDI2_TX1_DP	12	DDI2_TX3_DP
	13	DDI2_TX1_DN	14	DDI2_TX3_DN
	15	GND	16	DP1_CONFIG1
	17	DDI2_AUXP	18	DP1_CONFIG2
	19	DDI2_AUXN	20	DP1_HPD

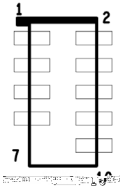
	1	DP2_PWR	2	DP2_PWR
	3	GND	4	GND
	5	DDI3_TX0_DP	6	DDI3_TX2_DP
	7	DDI3_TX0_DN	8	DDI3_TX2_DN
	9	GND	10	GND
	11	DDI3_TX1_DP	12	DDI3_TX3_DP
	13	DDI3_TX1_DN	14	DDI3_TX3_DN
	15	GND	16	DP2_CONFIG1
	17	DDI3_AUXP	18	DP2_CONFIG2
	19	DDI3_AUXN	20	DP2_HPD

5.8.3 CLR_CMOS1

	1	NC ثم
	2	PCH_RTCRST_N
	3	GND

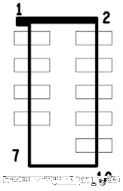
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5.8.10 COM3



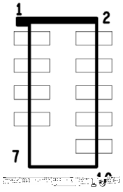
1	COM3_SIN	2	COM3_DCD
3	COM3_DTR	4	COM3_SOUT
5	COM3_DSR	6	GND
7	COM3_CTS	8	COM3_RTS
		10	COM3_RI

5.8.11 COM4



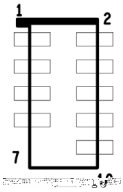
1	COM4_SIN	2	COM4_DCD
3	COM4_DTR	4	COM4_SOUT
5	COM4_DSR	6	GND
7	COM4_CTS	8	COM4_RTS
		10	COM4_RI

5.8.12 COM5



1	COM5_SIN	2	COM5_DCD
3	COM5_DTR	4	COM5_SOUT
5	COM5_DSR	6	GND
7	COM5_CTS	8	COM5_RTS
		10	COM5_RI

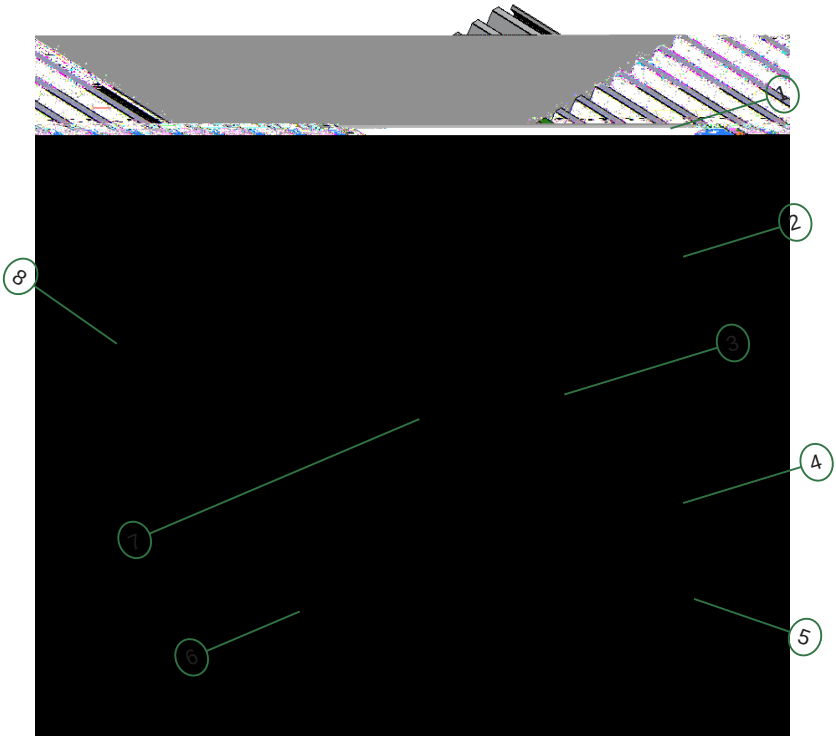
5.8.13 COM6



1	COM6_SIN	2	COM6_DCD
3	COM6_DTR	4	COM6_SOUT
5	COM6_DSR	6	GND
7	COM6_CTS	8	COM6_RTS
		10	COM6_RI

6

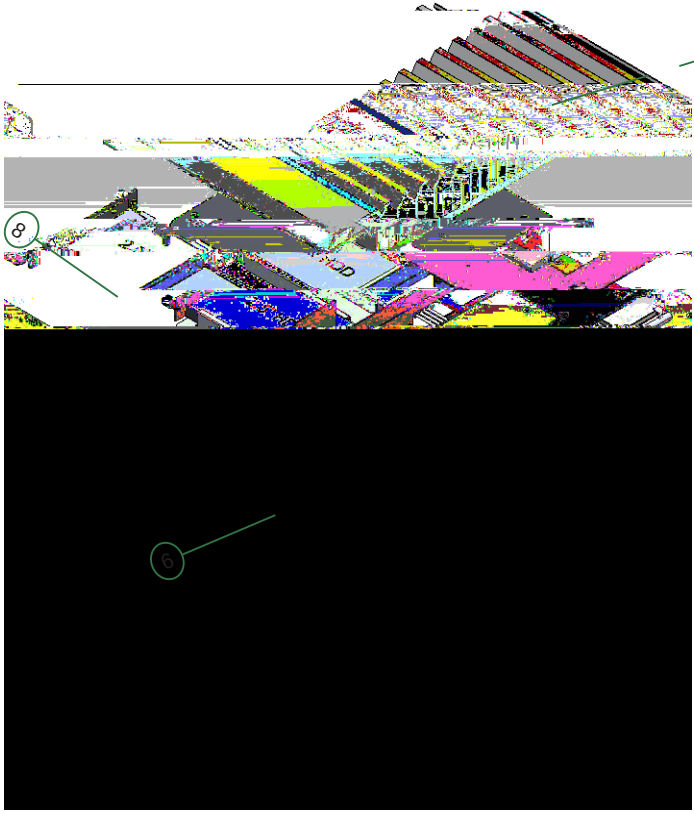
6.1 JMC-7310



1		2		3	CPU
4		5		6	
7		8	SATA		

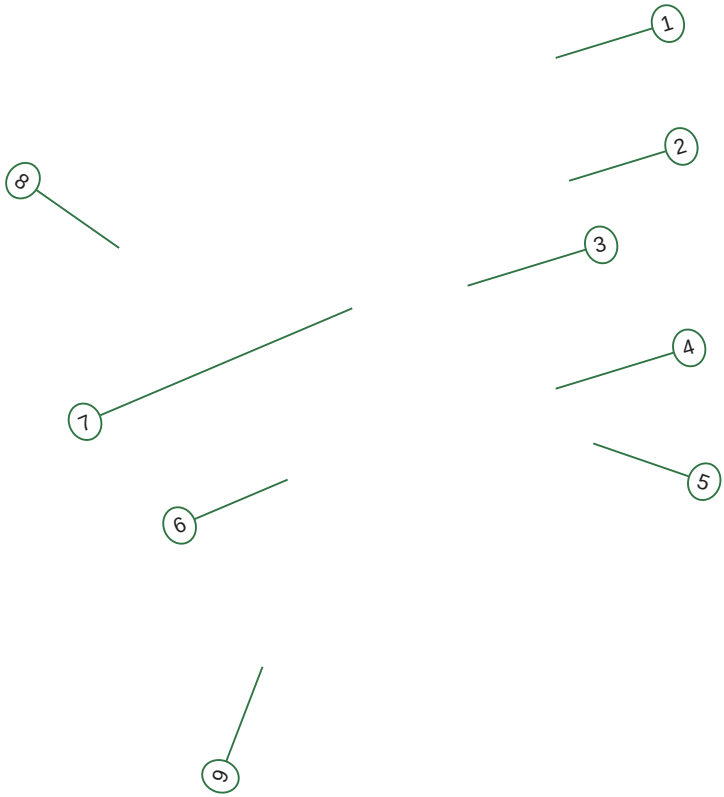
1		2		3	CPU
4		5		6	
7		8	SATA		
9	(1 x PCIex] Ⅵ = يتdž я لي Ā я @ œf1				

6.3 JMC-7312



1		2		3	CPU
4		5		6	
7		8	SATA		
9	(2 x PCI/1 x PCIex16+1 x PCI/1 x PCIex16+1 x PCIex4)				

6.4 JMC-7313



1		2		3	CPU
4		5		6	
7		8	SATA		
9	(1 x PCIex16+2 x PCI)				

6.5 JMC-7314



1		2		3	CPU
4		5		6	
7		8	SATA		
9	(1 x PCIex16+2 x PCI+1 x PCIex4)				

7 BIOS

7.1 BIOS

AMI BIOS BIOS Basic Input Output System (
ROM Read-Only Memory) BIOS

a. POST(Power On Self Test)
b.
c.
d. SETUP
BIOS CMOS RAM
BIOS CMOS
BIOS

7.2 BIOS

BIOS Setup BIOS

SETUP

a. SETUP
b.

BIOS BIOS

7.2.1 BIOS

<DEL> BIOS





7.2.2

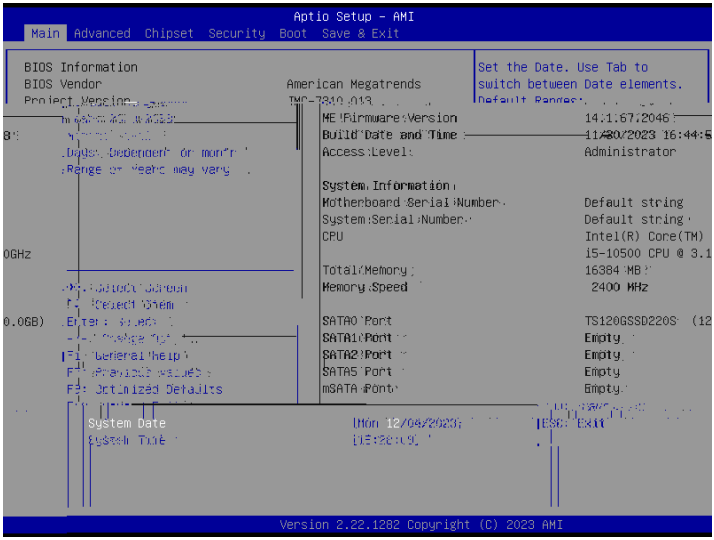
<Enter> <F1> <Esc>

← / →	
↑ / ↓	
+/ -	/
<Enter>	
<ESC>	CMOS SETUP
<F1>	
<F7>	
<F9>	
<F10>	CMOS

7.3 BIOS

Main		BIOS
Advanced		BIOS
Chipset		
Security		
Boot		

7.4 Malq



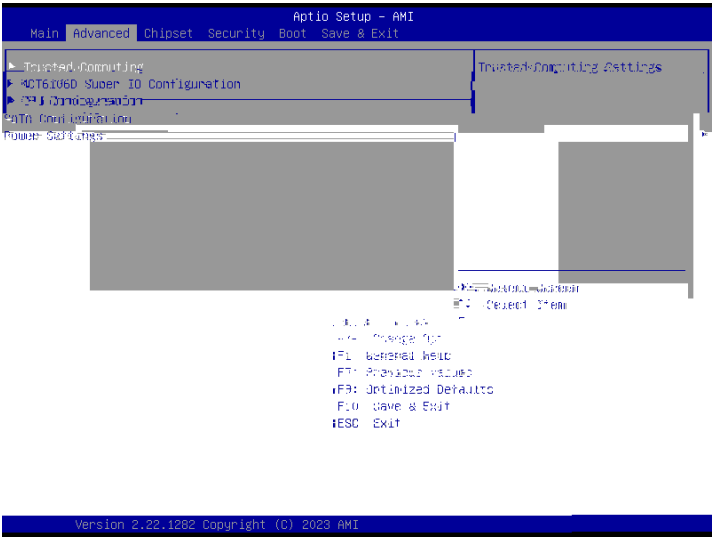
S|vwhp Dawh ( )

, “ , / / ”

S|vwhp Tlph

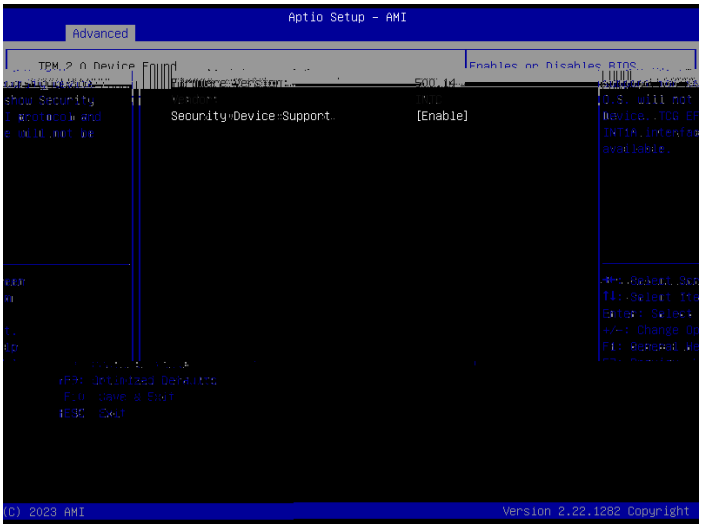
< >< >< >

7.5 Agyaqfhg



Tuxvwhg Crpsxwlqj		
NCT6106D Sxshu IO Crq jxudwlrq	Super IO	
CPU Crq jxudwlrq	CPU	
SATA Crq jxudwlrq	SATA	
Przhu Crq jxudwlrq		

- Trusted Confguration <Enter>

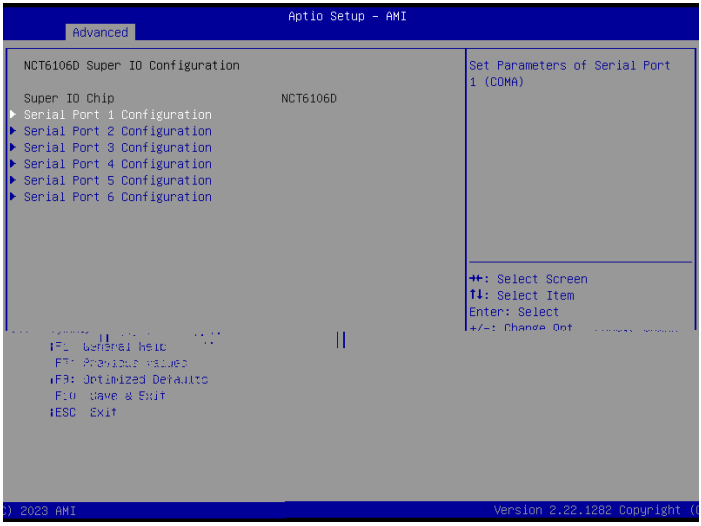


Shfxulw| Dhylfh Sxssruw

BIOS

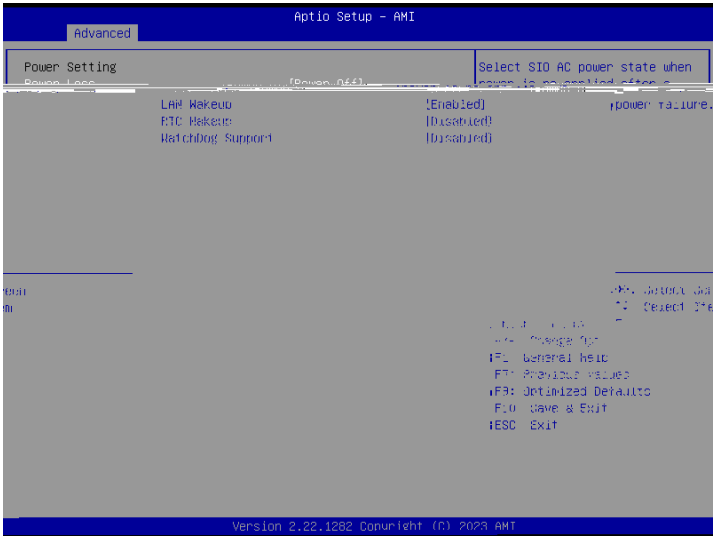
Disable,Enable.

- NCT6106D Super IO Confguration <Enter>



Shula0 Pruw 1/2/3/4/5/6 Crq jxuawlrq

- Power Configuration <Enter>



Przhu Lrvv

/ / AC

Power Of ,Power On,Last State.

LAN Wanhxs

Disable,Enable.

RTC Wanhxs

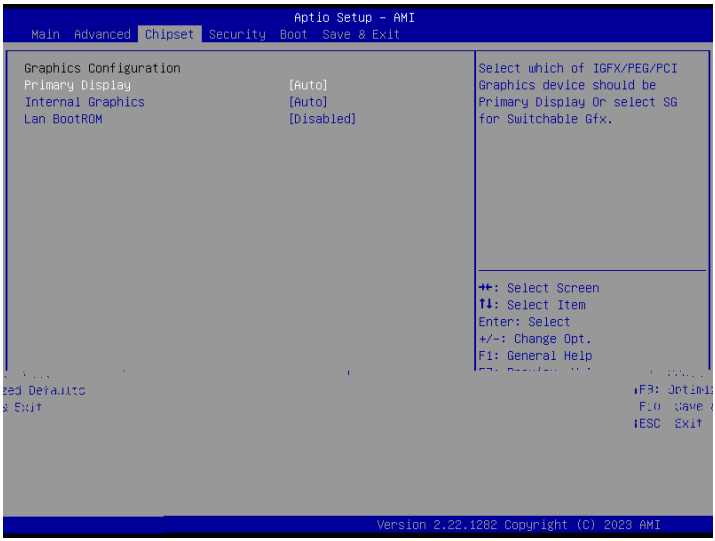
RTC

Disable,Enable.

WawfkDrj Sxssruw

Disable,Enable.

7.6 CkIsvhW



Pul p au| Dlvs◦a|

Auto,IGFX,PEG.

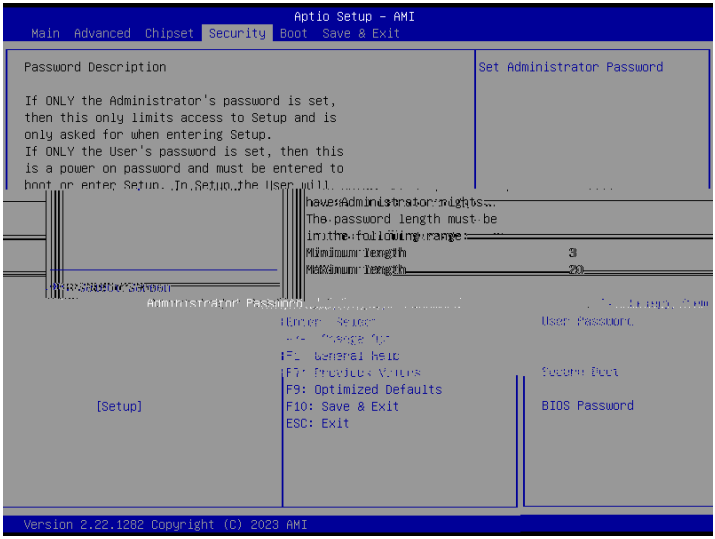
Iqwhuqa◦ GuaskIfv

Auto,Disable,Enable.

Laq Br rwROM

Disable,Enable.

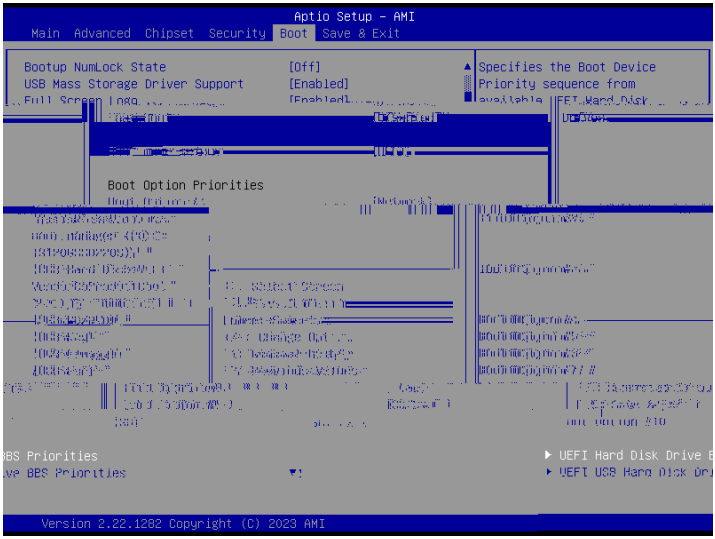
7.7 Shfxulw|



Ag p lqlvwudwru Pavvz rug

1. Administrator Password <Enter>
2. “ Create New Password ” 3~20 g,

7.8 Brrw



Brrw Nxp Lrfn Swawh

NumLock

On,Of.

USB Mavv Swrua j h Dulyhu Sxss ruw

USB

Disable,Enable.

Fxoo Sfuhhq Lr j r

Logo

Disable,Enable.

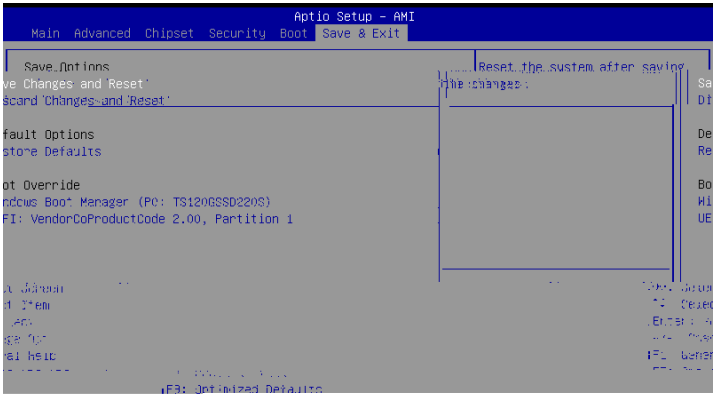
Favw Brrw

Disable,Enable.

Brrw Oswlrq #1-10

NVME,Hard Disk,USB Hard Disk,USB key,USB CD/DVD,Network,UEFI AP: Built-in EFI Shell.

7.9 Sayh&E{lw



Sayh Ckaqjhv aqg Rhvhw

Dlvfaug Ckaqjhv aqg Rhvhw

Rhvwruh Dhiaxowv

8

JMC-7310 GPIO

8.1 GPIO

JMC-7310 GPIO
1 GPIO0 GP30/31/32/33/34/35/36/37 /
2 GPIO1 GP40/41/42/43/44/45/46/47 /
3 GPIO Group GP3x/4x Logical Device 7
4 GP3x(30~37) / Logical Device 7 CR 0xEC Bit0~Bit7 0: Output Pin / 1:Input Pin
GP4x(40~47) / Logical Device 7 CR 0xF0 Bit0~Bit7 0: Output Pin / 1:Input Pin
GP3x(30~37) Logical Device 7 CR 0xED Bit0~Bit7
GP4x(40~47) Logical Device 7 CR 0xF1 Bit0~Bit7
5 GPIO Group3 GPIO Group4 GPIO_GROUP_3_IO_REGISTER/GPIO_GROUP_3_DATA_REGISTER GPIO Group4 0x30/0x37 0x40/0x47

```
#define SuperIo_Index_Port 0x2E
#define SuperIo_Data_Port 0x2F
#define GPIO_LDN7_DEVICE 0x07
#define GPIO_GROUP_3_IO_REGISTER 0xEC
#define GPIO_GROUP_4_IO_REGISTER 0xF0
#define GPIO_GROUP_3_DATA_REGISTER 0xED
#define GPIO_GROUP_4_DATA_REGISTER 0xF1

GPIO Gurxs 3 LL
//a. Sxshu IO Crq jxuawlrq Mrgh
IoWrite8(SuperIo_Index_Port, 0x87);
IoWrite8(SuperIo_Index_Port, 0x87);

//b. GPIO, LDN 7
IoWrite8(SuperIo_Index_Port, 0x07);
IoWrite8(SuperIo_Data_Port, GPIO_LDN7_DEVICE);

//f. GPIO GP3{(30¢37) Iqsxw Plq
IoWrite8(SuperIo_Index_Port, GPIO_GROUP_3_IO_REGISTER);
IoWrite8(SuperIo_Data_Port, 0xFF); //0xFF GPIO GP3x(30~37) Input Pin

//g. GPIO Gurxs 3 GP33
UINT8 BitOfset = 3;
UINT8 Data8
IoWrite8(SuperIo_Index_Port, GPIO_GROUP_3_DATA_REGISTER);
Data8 = IoRead8(SuperIo_Data_Port);
Data8 = Data8 >> BitOfset;
Data8 = Data8 & 0x1;
if (Data8){
return 1;// GPIO
```

```
}else{
  return 0;//       GPIO
}

//h.      GPIO GP3{(30¢37)    Oxwsxw Plq
IoWrite8(SuperIo_Index_Port, GPIO_GROUP_3_IO_REGISTER);
IoWrite8(SuperIo_Data_Port, 0x00); //0x00       GPIO GP3x(30~37)              Output Pin

//i.    GPIO Gurxs 3                    GPO              GPIO              GPI              Щ
for(GpioNumber=0x30; GpioNumber <= 0x37; GpioNumber++)
{
BitOfset = GpioNumber - 0x30;
IoWrite8(SuperIo_Index_Port, GPIO_GROUP_3_DATA_REGISTER);
Data8 = IoRead8(SuperIo_Data_Port);
Data8 &=~(0x1 << BitOfset);//       bit       0          GPIO
//Data8 |= (0x1 << BitOfset); /*       bit          1          GPIO              */
IoWrite8(SuperIo_Data_Port, Data8);//
}
//g.       Super IO    Confguration Mode
 IoWrite8(SuperIo_Index_Port, 0xAA); //       Super IO Confguration Mode       SuperIO
                        ,                  Confguration Mode
```

8.2 WDT

```
#defne SuperIo_Index_Port 0x2E
#defne SuperIo_Data_Port 0x2F
#defne GPIO_LDN8_DEVICE 0x08
UINT8 Data8

//a.       Sxshu IO    Crq   jxuawlrq Mrgh
IoWrite8(SuperIo_Index_Port, 0x87);
IoWrite8(SuperIo_Index_Port, 0x87);

//b.                    GPIO, LDN 8
IoWrite8(SuperIo_Index_Port, 0x07);
IoWrite8(SuperIo_Data_Port, GPIO_LDN8_DEVICE);

//f. Eqabohg WDT
IoWrite8(SuperIo_Index_Port, 0x30);
IoWrite8(SuperIo_Data_Port, IoRead8(SuperIo_Data_Port) | 0x01);

//g.       WDT                          Rhjlvwhu 0{F0    Blw3          1                    0
IoWrite8(SuperIo_Index_Port, 0xF0);

//
IoWrite8(SuperIo_Data_Port, IoRead8(SuperIo_Data_Port) | 0x08);

//
// IoWrite8(SuperIo_Data_Port, IoRead8(SuperIo_Data_Port) & 0xF7);
```

```
  //h.      WDT              5   /
   IoWrite8(SuperIo_Index_Port, 0xF1);
   IoWrite8(SuperIo_Data_Port, 0x5);

   //i.      SxshuIO  Crq  jxuawlrq Mrgh
   IoWrite8(SuperIo_Index_Port, 0xAA);

    //      SxshuIO Crq  jxuawlrq Mrgh      SxshuIO                    ,
Crq  jxuawlrq MrghЩ
```

9

9.1

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